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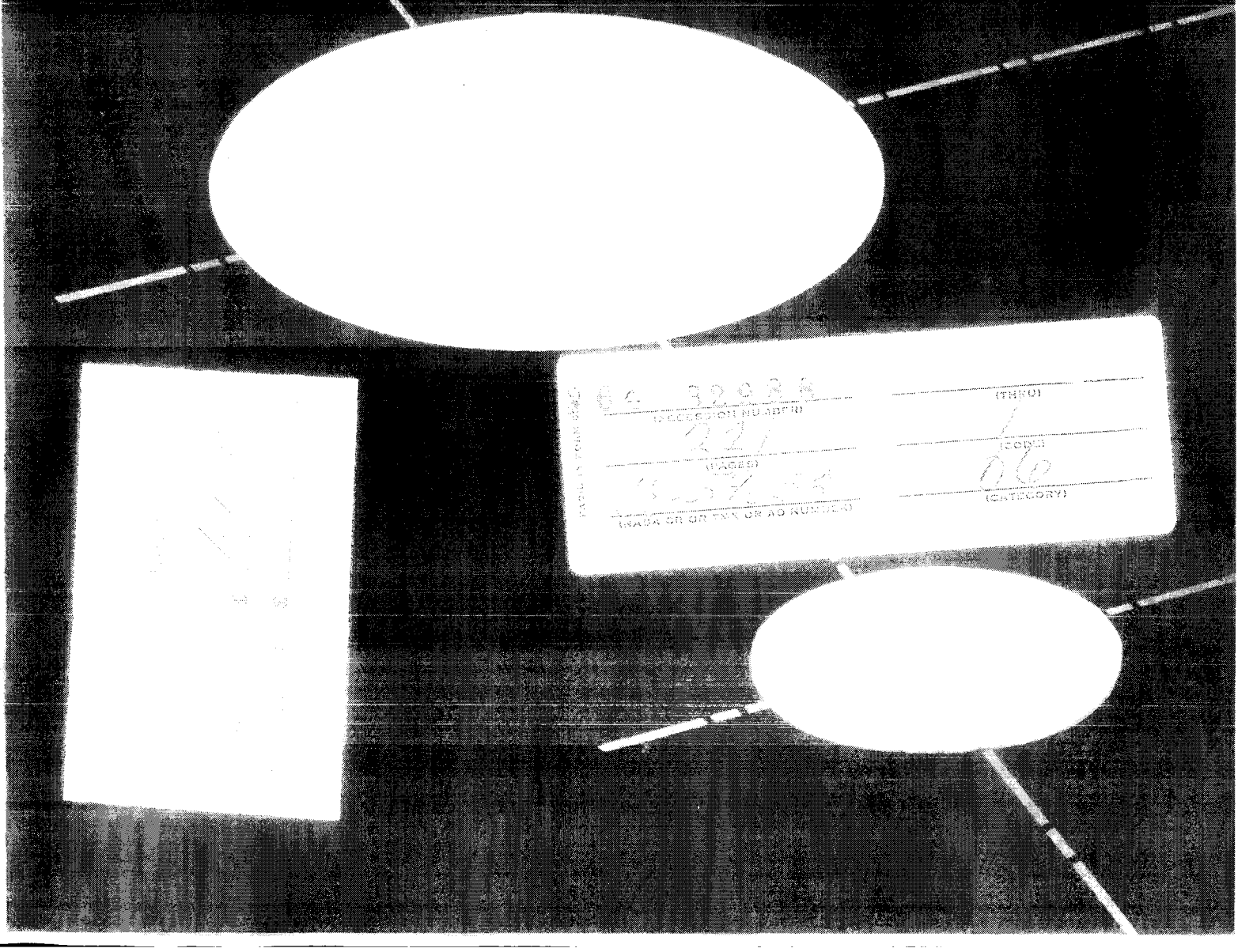

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A Digital Compensator For Automatic Control Systems

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by

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ABSTRACT

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A full adder-subtractor utilizing one transistor in the carry-borrow signal path is presented. This circuit is incorporated in an arithmetic unit which performs addition, subtraction, multiplication and division. The unique arithmetic unit, in turn, is incorporated in a multi-increment digital integrator. By means of a magnetic drum memory unit, the one arithmetic unit is time shared among 18 integrators. The 18 integrators are designed into a digital compensator for a simulated plant. The one digital compensator, in turn, can be time shared to control many plants simultaneously.

A current mapping technique for implementing the circuit logic is presented. A digital to a-c converter is developed.

The integrands are constants in the digital integrators of the compensator. In this case there is no truncation error and the round-off error can be reduced to any desired magnitude in the multi-increment integrator design presented. A non-linear saturation circuit obtains the maximum speed from the plant when the linear range is exceeded.

An "ideal" program for the digital compensator is synthesized for the simulated plant as an example of the use of the compensator. The "ideal" program is based upon minimizing Wieners mean square error functional.

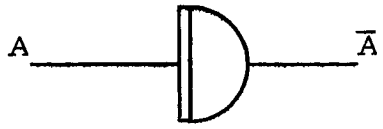
Complete construction details for the compensator designed are presented.

ACKNOWLEDGEMENTS

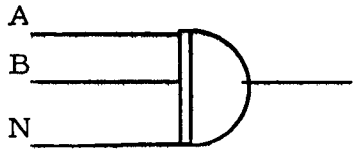
The author wishes to express his deep appreciation to Professor Harry W. Mergler, Director of the Digital Systems Laboratory of the Case Engineering Design Center, for his encouragement and guidance in the conduct of this investigation. The author is also indebted to the National Aeronautics and Space Administration for financially supporting the research. I am grateful to Dean Stuart Johnson, and Professors Herbert Lissner, George Loweke and Edward Zobel of Wayne State University and Professor George Uicker of the University of Detroit for their support in obtaining for me a National Science Foundation Faculty Fellowship which made my doctoral studies financially possible. I express my deepest gratitude and love for my wife, Phylis J. Kearns, who assumed my home duties to give me time and a free mind to study. I would also like to acknowledge the assistance given by the staff of the Engineering Design Center and by my fellow graduate students in the Digital Systems Group.

KEY TO SYMBOLS AND NOTATIONS

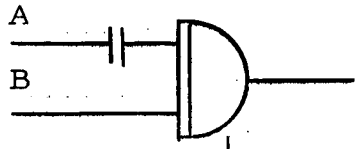
Logic Symbols



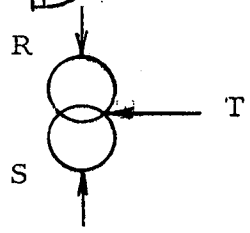
NOR 1 or INVERTER



$\overline{A+B+\ldots+N}$ NOR-N GATE

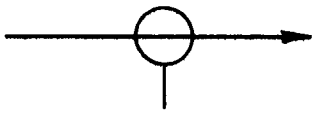


$\overline{A+B}$ GATED PULSE GENERATOR
(USED AS NOR-2)

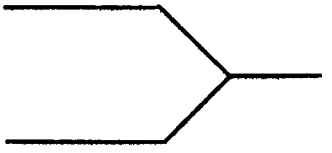


RESET-SET-TRIGGER MEMORY UNIT
(flip-flop)

ONE SHOT MULTIVIBRATOR



STEERING GATE



DIGITAL INTEGRATOR

Notation

x(t)	Continuous function in the variable time.
x(nt)	Either a continuous or discreet function in the variable time but the value is examined only at integral multiples of T.
s	Laplace transform variable.

Z	Z-transform calculus variable
ΔZ	Overflow register in a digital integrator
bit	The information in one memory unit of the compensator in the form of a ZERO or ONE.
word	A number of bits are grouped together in the same context and treated as a unit.
quantize	If a continuous variable is approximated by a series of magnitudes that cannot differ from one another by less than some least interval, the variable is said to be "quantized".
plant	a general term for any control system to be assisted by the compensator.

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I. INTRODUCTION

Automatic controls are developed to perform many specific tasks. The control of position, velocity, temperature, pressure, etc. are examples of physical quantities to be controlled. The control engineer may be told what power media and basic system components to use. He may also be given a specification for the desired system performance. System components are chosen from those that are available and economical. The performance specification relates to the stability, accuracy and speed of response. Normally a system gain adjustment is not sufficient to achieve the desired performance. When modification of the basic elements is not possible or economical, the system performance can be changed by adding a compensating element to the system. The design of the compensating element could be considered the essence of design since it is required to overcome the deficiencies of the basic elements and to make the overall performance acceptable.

This thesis is concerned with the design of such a compensator for a digital automatic control system. For the overall system to possess a high speed of response, the compensator must possess a high speed of response. Unique logical circuitry for the arithmetic operations is developed and incorporated in a multi-increment integrator which is designed to possess a high speed of response.

In some analog systems, for example, a tachometer might be added to the gear train of a position servomechanism to provide a proper amount of system damping. Since the tachometer possesses inertia it reduces the potential dynamic performance of the system and also increases cost. Here, the compensation is achieved numerically so only the minimal plant system is required. Since the controlled variable is a shaft position in this thesis the minimal plant consists of a motor and associated gear train. This minimal system can represent many varied systems since to use the compensator it is only necessary to digitize the controlled variable.

A system block diagram is shown in Fig. 1-1. The plant consists of a servoamplifier, motor, gear train, and load. An absolute-data digital encoder mounted on the controlled variable provides feedback information in digital form. The compensator consists of a compensator unit, the numerical compensation unit and a digital to A-C sample and hold unit.

To make the compensator economical, it is designed to make the computations quickly, so that one compensator can be time shared among many separate control systems.

To make the compensator versatile the compensator is provided with a reserve internally stored program which can be switched into the system to alter the plant performance.

An introduction to sampled-data theory is presented in chapter II. In chapter III the specification for the "ideal" plant compensator is given. In chapter IV a basic system block diagram is developed and the function of each unit explained. A detailed design of each unit is presented in chapter V. Many auxiliary features are required in a control unit to facilitate the use of the compensator. These auxiliary circuit features are presented in chapter VI. Experimental results and design verifications are given in chapter VII. Recommendations for future work are given in chapter VIII.

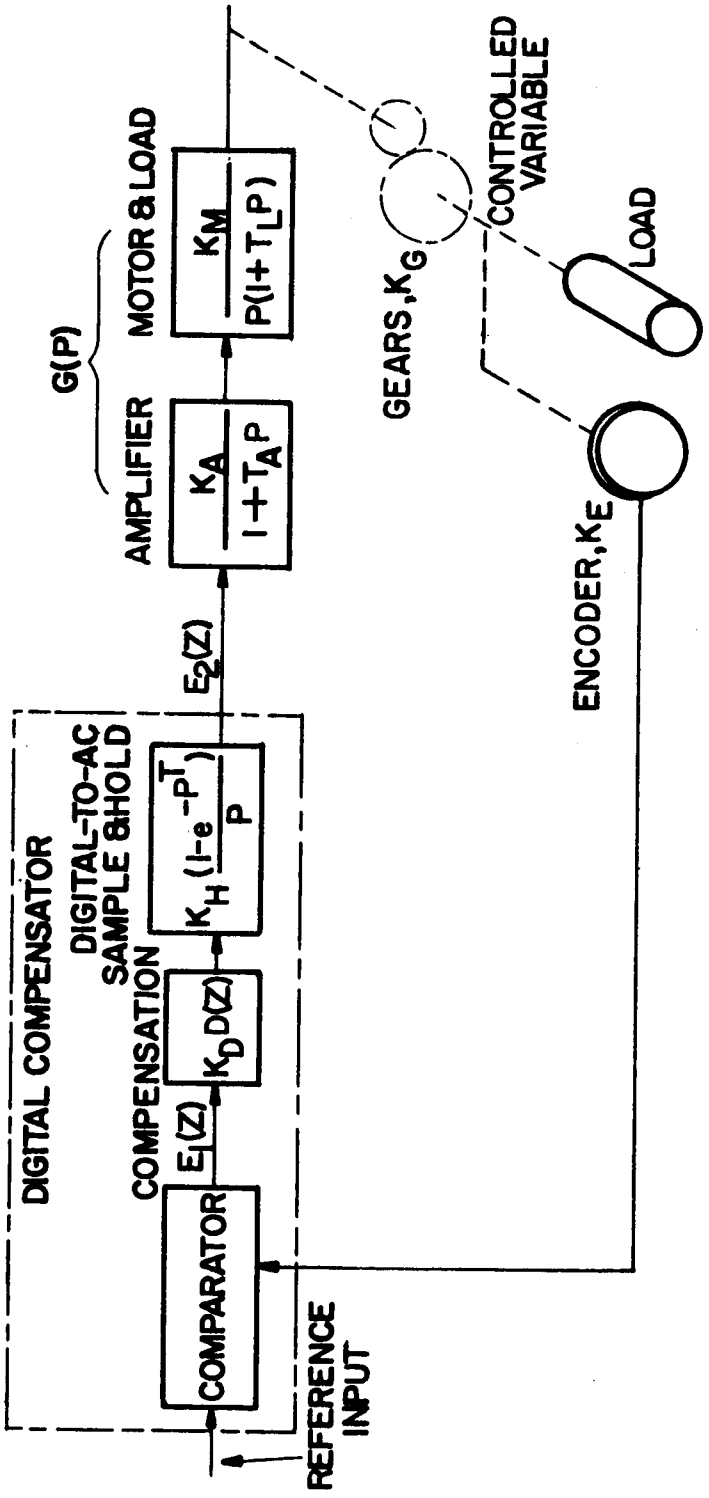


FIGURE 1-1 MATHEMATICAL SYSTEM BLOCK DIAGRAM

II. INTRODUCTION TO SAMPLED DATA THEORY

The absolute-data encoder mounted on the shaft shown in Fig. (1-1), converts the shaft position information into a digitized form as shown in Fig. (2-1). The height of each step depends upon

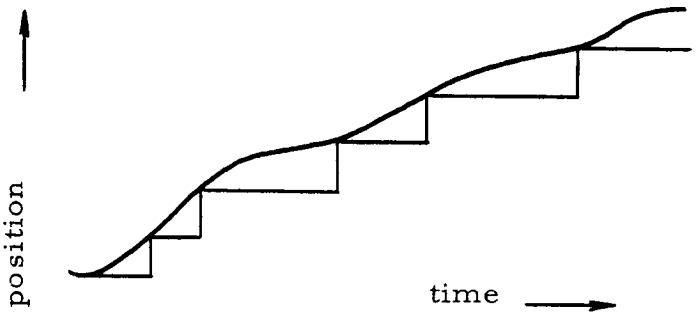


Fig. (2-1) - Analog to digital conversion of shaft position.

the encoder resolution (quanta) and the length of each step depends upon the amount of time the shaft position is within a quantum. The encoder converts the analog shaft position into a discrete digital word.

To form the actuating error, $E_1(Z)$ in Fig. (1-1), the controlled variable word is subtracted from the reference variable word. The amount of time allotted in the compensator to detect these words is 12 μ sec. The period of time between the computation of successive actuating errors is 18 millisec. Thus it can be seen that the actuating error used in the compensator is only a sampling of the physically continuous actuating error. Let the continuous signal be x(t) and assume we are sampling x(t) at t=0, +T, +2T, ... +nT, i.e. periodically at equal time intervals T. We will denote the value of x(t) at the n^{th} time interval by x(nT).

Due to the ratio of detecting time to sampling time, the sampled signal derived from x(t) may be thought of as a train of pulses of height x(nT) and of infinitesimal duration. But because each of these

pulses has zero area, a linear system will not respond to them. Accordingly, we will use another circuit which will take the sampled magnitude x(nT) and hold that magnitude for the sample period. Thus, x(nT) exists physically only within the compensator. x(nT) does not appear physically in the servomechanism, it is just a mathematical procedure for representing part of the clamping process.

Mathematically we shall consider the sampled signal x(t) at the sample instant nT as consisting of a delta function proportional to the sampled value of x(t) at that n. The resulting train of impulses constitutes what we shall denote as x*(t), the sampled input function obtained from x(t). Thus,

$$x^*(t) = x(t)\,\delta_T(t) = \sum_{n=-\infty}^{\infty} x(nT)\,\delta\,(t-nT) \qquad (2\text{-}1)$$

where $\delta_T(t)$ is a train of unit impulses defined by

$$\delta_T(t) = \sum_{n=-\infty}^{\infty} \delta(t-nT) \qquad (2\text{-}2)$$

The various waveforms are illustrated in Fig (2-2). In order to obtain a staisfactory graphical representation, it was necessary to plot the pulses with a finite height and width.

To obtain an alternate expression for $x^*(t)$ in the frequency domain, we may take the Fourier Transform of eqn. (2-2).

$$X^*(j\omega) = \sum_{n=-\infty}^{n=\infty} x(nT) \int_{-\infty}^{\infty} \delta(t-nT)\quad e^{-j\omega t}dt$$

$$= \sum_{n=-\infty}^{\infty} x(nT)\ e^{-jn\omega T} \int_{-\infty}^{\infty} \delta(t-nT)dt$$

$$= \sum_{n=-\infty}^{\infty} x(nT)\ e^{-jn\omega T} \qquad (2\text{-}3)$$

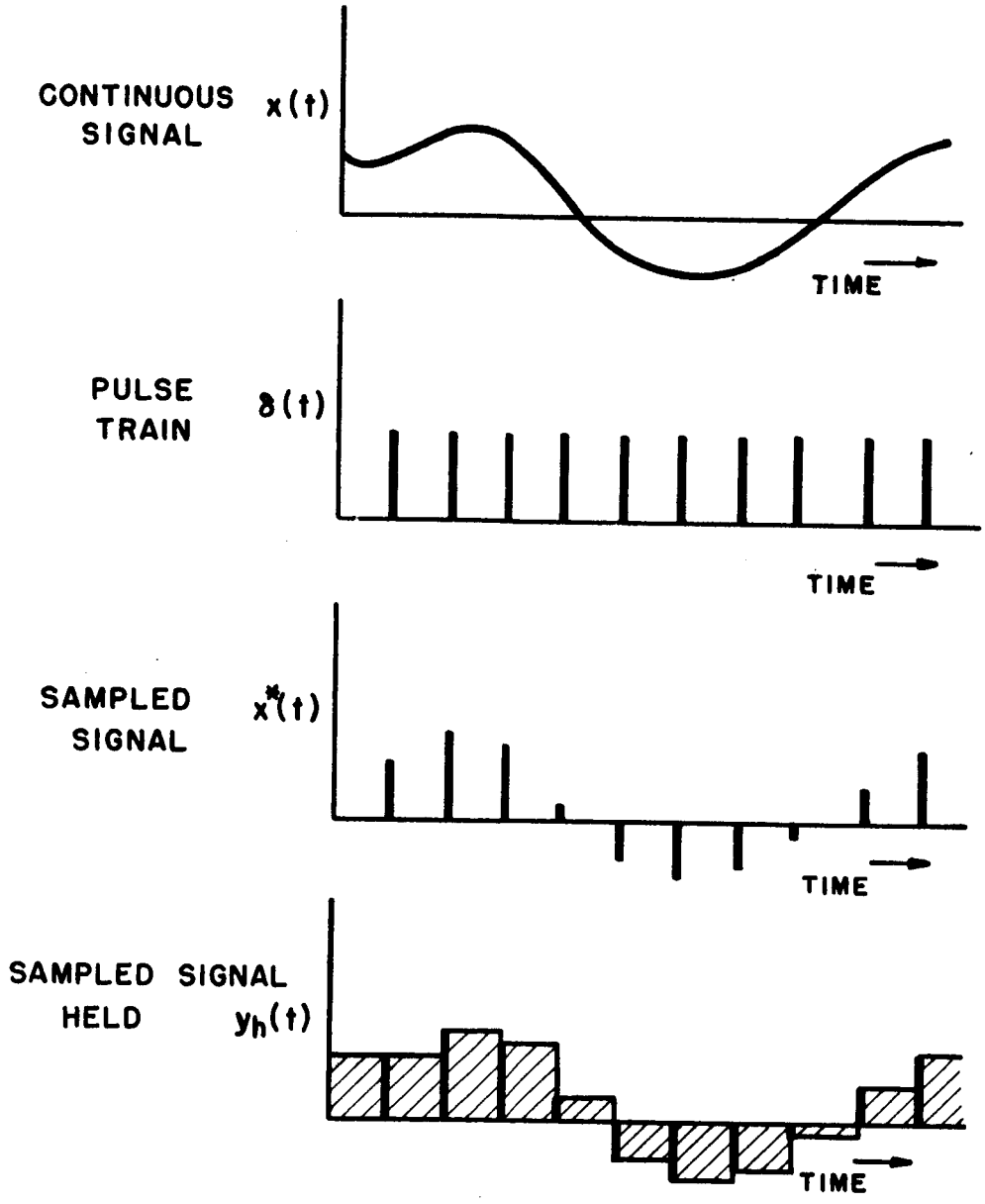


FIGURE 2-2 SYSTEM WAVEFORMS

This expression for the pulsed transfer function $X^*(j\omega)$ can be simplified b defining a new variable Z which is related to $j\omega$ by the formula

$$Z = e^{j\omega t} \tag{2-4}$$

In terms of the Z variable, the pulsed transfer function $X^*(j\omega)$ can be written

$$X^*(Z) = \sum_{n=0}^{\infty} x(nT)\, Z^{-n} \tag{2-5}$$

where we have written Y^* as a function of Z rather than ω. Actually since $j\omega = \frac{\ln Z}{T}$, X^* should be written

$X^*\left(\frac{\ln Z}{T}\right)$, but for convenience, we write $X^*(Z)$.

Consider Fig. 2-3 where the continuous input signal is turned into a pulsed signal $X^*(t)$ by the sampling operation. The pulsed signal is the input to the linear system with transfer function $G(j\omega)$. The output of the linear system is the continuous signal $c(t)$. However our actuating error is obtained by sampling $c(t)$ at the same time $x(t)$ is being sampled. For our particular purposes, and sampled data theory in general, we desire to consider the output $c(t)$ only at the sample instants (nT).

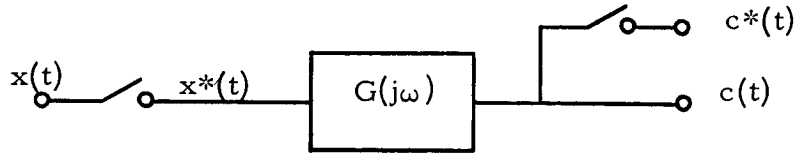


Fig. (2-3) - Sampled system notation.

The Fourier transform $C(j\omega)$ of the continuous output $c(t)$ is given by

$$C(j\omega) = X^*(j\omega)\, Y(j\omega) \tag{2-6}$$

The sampled signal can be thought of as an infinite number of amplitude-modulated carriers, the frequency of successive carriers being separated by the sample frequency ω_T. The modulating signal is simply x(t). From this consideration

$$X^*(j\omega) = \frac{1}{T} \sum_{n=-\infty}^{\infty} X(j\omega + jn\omega_T) \qquad (2\text{-}7)$$

But we desire $C^*(j\omega)$

$$\therefore C^*(j\omega) = \frac{1}{T} \sum_{n=-\infty}^{\infty} C(j\omega + jn\omega_T) = X^*(j\omega) \frac{1}{T} \sum_{n=-\infty}^{\infty} Y(j\omega + jn\omega_T)$$

$$\text{or} \quad C^*(j\omega) = X^*(j\omega)\, Y^*(j\omega) \qquad (2\text{-}8)$$

$$\text{where} \quad Y^*(j\omega) = \frac{1}{T} \sum_{n=-\infty} Y(j\omega + jn\omega_T)$$

The important point here is that $Y^*(j\omega)$ is the transfer function of the linear system when the input is sampled and the output is considered sampled. That is, the frequency spectrum of the pulsed output can be obtained from the frequency spectrum of the pulsed input simply by multiplication of the input spectrum by $Y^*(j\omega)$.

Since, the system uses a sample and hold circuit, we need to compute its transfer function, that is, the transfer function which produces $y_h(t)$ from $x^*(t)$.

$$Y_h(jW) = \int_0^{\infty} W(t)\, e^{-j\omega t} dt \qquad (2\text{-}9)$$

where W(t), the unit impulse response corresponding to this transfer function, must convert an impulse of area x(nT) into a pulse of width T and height x(nT). Thus,

$$W(t) = 1 \qquad 0 \leq t < T$$
$$W(t) = 0 \qquad t > T$$

The Fourier Transform of W(t) is the transfer function $Y(j\omega)$ and is calculated as follows:

$$Y_h(j\omega) = \int_0^\infty w e^{-j\omega t}dt = \int_0^T e^{-j\omega t}dt$$

$$= -\frac{1}{j\omega} e^{-j\omega t}\Big|_0^T$$

$$= \frac{1 - e^{-j\omega T}}{j\omega} \qquad (2\text{-}10)$$

In terms of the operator p, we replace $j\omega$ by p, and obtain

$$Y_h(p) = \frac{1 - e^{-pt}}{p} \qquad (2\text{-}11)$$

We can obtain G*(Z) for sampled and held inputs by obtaining the Z transform of

$$G(p)_h = Y_h(p)G(p) \qquad (2\text{-}12)$$

$$G^*(Z) = Z\{Y_h(p)G(p)\} = Z\left\{\frac{1 - e^{-pt}}{p} G(p)\right\}$$

$$= Z\left\{\frac{G(p)}{p}\right\} - Z\left\{\frac{e^{-pt}G(p)}{p}\right\} \qquad (2\text{-}13)$$

To evaluate the last term, consider the Z transform of $e^{-pt}X(p)$. Since $e^{-pt}X(p)$ corresponds to the time function $x(t-T)$

$$Z\left\{e^{-pt}X(p)\right\} = \sum_{n=-\infty}^{\infty} x(nT-T)Z^{-n} = \sum_{n=-\infty}^{\infty} x(nT)Z^{-n-1}$$

$$= Z^{-1}Z\{X(p)\} \qquad (2\text{-}14)$$

Placing this intermediate result in eqn. (1-13), we obtain

$$G^*(Z) = Z\left\{\frac{G(p)}{p}\right\} - Z^{-1}Z\left\{\frac{G(p)}{p}\right\}$$

$$= (1-Z^{-1})Z\left\{\frac{G(p)}{p}\right\} \qquad (2\text{-}15)$$

We are now in a position to write the open loop transfer function equation for the plant which includes the sample-and-hold circuitry. The block diagram of the system is shown in Fig (1-1).

The digital controller performs the comparison operation and makes the necessary calculations to compensate the system. The output of the digital controller is then held for a sample period and converted to an amplitude modulated 60cps carrier waveform by the digital-to-ac converter. The servoamplifier provides gain to the system and power to the servomotor. The frequency response of the servoamplifier is given in Fig 5-16. The low frequency response is down 3db at 10cps. Accordingly, the frequency response about the 60cps carrier frequency is 50cps. Thus

$$T_A = \frac{1}{\omega_A} = \frac{1}{2\pi F_A} = \frac{1}{2\pi 50} = 0.003 \text{ sec.} \qquad (2\text{-}16)$$

The frequency response of the servomotor with load is given in Fig 60. The response breaks at 3.5cps. Thus

$$T_L = \frac{1}{\omega_A} = \frac{1}{2\pi F_L} = \frac{1}{2\pi(3.5)} = 0.045 \text{ sec.} \qquad (2\text{-}17)$$

Let

$$K = K_D K_H K_A K_M K_G K_E$$

where K_D = digital controller gain, #/#
K_H = sample and hold gain, volts/#
K_A = amplifier gain, volts/volt
K_M = motor gain, rad/sec/volt (2-18)
K_G = gear train gain, radian/radian
K_E = encoder gain, #/radian

The units of K are

$$\frac{\text{No.}}{\text{No.}} \cdot \frac{\text{volts}}{\text{No.}} \cdot \frac{\text{volts}}{\text{volt}} \cdot \frac{\text{rad/sec.}}{\text{volt}} \cdot \frac{\text{radian}}{\text{radian}} \cdot \frac{\text{No.}}{\text{radian}} = \text{sec}^{-1}$$

G(p) for the servomechanism in this system has the following form:

$$G(p) = \frac{K}{p(1+T_A p)(1+T_L p)} \qquad (2\text{-}19)$$

Referring to eqn. (2-15).

$$\frac{G(p)}{p} = \frac{K}{p^2(1+T_A p)(1+T_L p)}$$

The Z transform for this system is derived in Appendix A. The result is rewritten here

$$(1-Z^{-1})Z\left\{\frac{G(p)}{p}\right\} =$$

$$= \frac{0.002290KZ^{-1}(1+1.4811Z^{-1})(1+0.0451Z^{-1})}{(1-Z^{-1})(1-.67Z^{-1})(1-.0025Z^{-1})} \qquad (2\text{-}20)$$

Before proceeding it is instructive to consider the locations of the values of Z in the complex Z plane which correspond to different values of the frequency ω. From

$$Z = ie^{j\omega T_r} = i(\cos \omega T + \sin \omega T) \qquad (2\text{-}21)$$

it is evident that the magnitude of Z is equal to one for all values of ω so that the values of Z all lie on the unit circle as shown in Fig (2-4). Corresponding to $\omega = 0,\ \omega_r,\ 2\omega_r, \ldots$ the Z plane value is (1, 0). Note that since $T = 1/\omega_r$ frequencies ω which differ by an integral multiple of the repetition frequency, ω_r, lie at the same point on the unit circle in the Z plane. Complementary frequencies ω_1 and ω_2 ($\omega_2 = -\omega_1$) are conjugate complex points in the Z plane.

Actually, there is no need to restrict $j\omega$ to purely imaginary values. Thus, let

$$Z = e^{sT_r} \qquad (2\text{-}22)$$

where $s = \sigma + j\omega$

When the real part of σ is zero, $s = j\omega$ and we are considering pure sinusoids. When the real part, σ, is negative we are considering exponentially decreasing sinusoids. The corresponding Z values of s lie inside the unit circle in the Z plane, since

$$Z = e^{sT_r} = e^{\sigma T_r}\, e^{j\omega T_r} \quad \text{and} \quad |Z| = e^{\sigma T_r} \qquad (2\text{-}23)$$

For a negative σ, $|Z| < 1$

When the real part of s is positive, we are considering exponentially increasing sinusoids. Therefore, the right half of

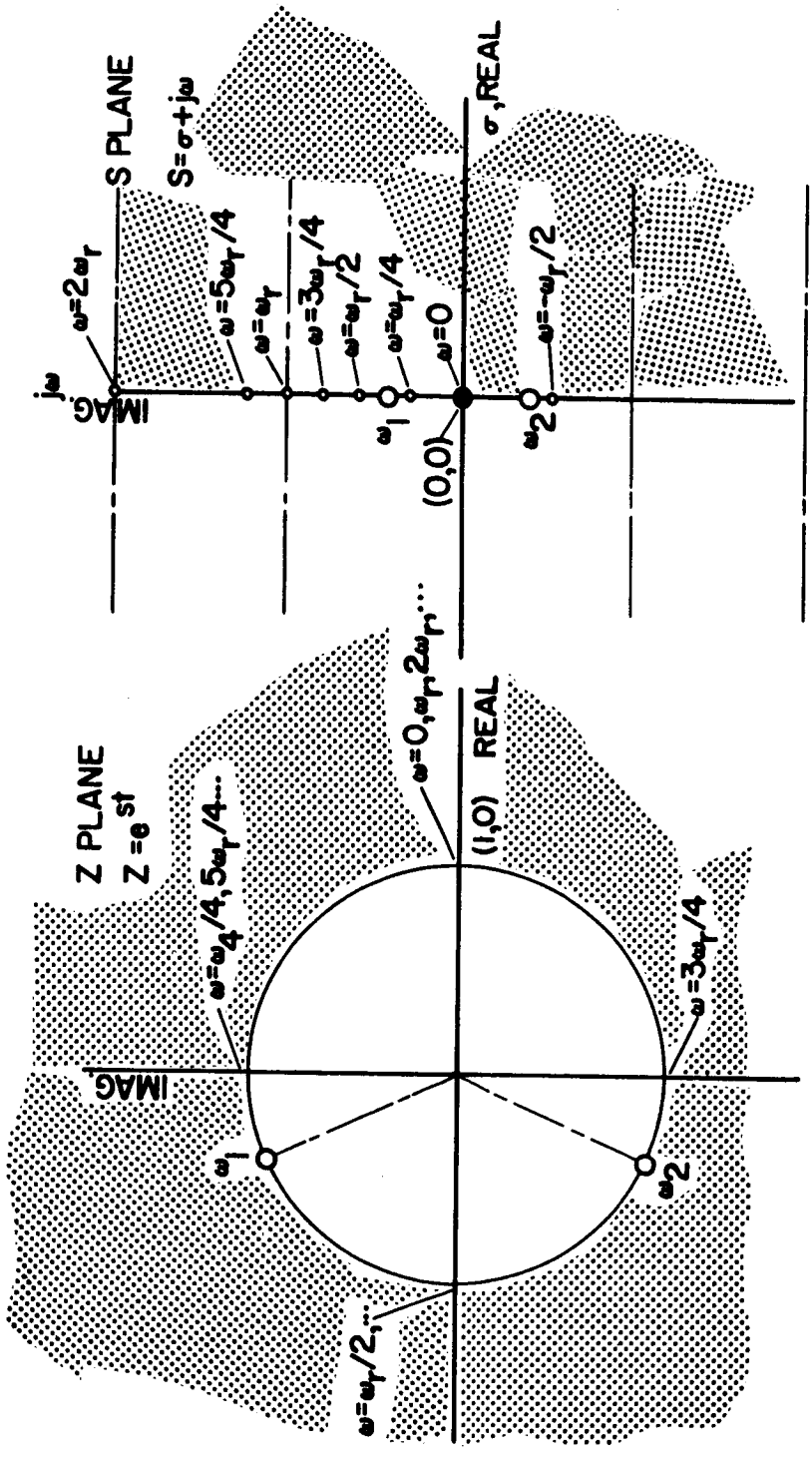


FIGURE 2-4 TRANSFORMATION OF S-PLANE TO Z-PLANE

the plane plots over to the region outside the unit circle in the Z plane. The corresponding regions are shown shaded in Fig (2-4).

A necessary condition for the stability of the closed-loop system is that none of the poles be located in the right half of the s-plane. A corresponding condition is that none of the poles of the closed loop system be located outside the unit circle in the Z plane.

Inspection of eqn. (1-20) indicates that the pulsed and held transfer function for the plant has a zero outside the unit circle and a pole on the unit circle in the Z plane.

III. COMPENSATION OF THE PLANT

The compensation of the plant is dependent upon the type of input expected and the performance desired. It is desired to compensate the plant, in some "ideal" sense. In a previous work,[1] the author compensated the accelerometers of an inertial navigation system by instrumenting the reciprocal of the accelerometer transfer function with analog active components which included filters. The compensation was placed in series with the instrument. A variety of cases were instrumented some being more "practical" than others. Also, the effects of noise on the compensated output were discussed. Since the compensation was used open-loop, there was no stability constraint except in the compensation unit itself. In this thesis, the matter of stability must also be included.

Let us specify our ideal system:

1) the system must be stable
2) the compensation must be physically realizable
3) the system response should be ripple-free
4) the response should possess a finite settling time
5) the steady state response should be error free
6) further, we require that the system minimizes the effects of white noise at the input.

Each of these requirements contributes a constraint on

the compensation design. In this chapter each of these requirements will be discussed from the point of view of how it effects the compensation design. A set of equations will be presented which must be satisfied simultaneously to meet the specification. This set of equations will be solved and the required compensation determined. In the next chapter, the method of physically realizing the compensation will be given.

Obviously, there are limits upon the performance which can be achieved due to the characteristics of the prime mover. For example, an infinite acceleration of the load cannot be achieved. There is more freedom in the manipulation of signals and information flowing in the system but saturation effects can limit even these manipulations.

One technique[2] for improving the overall transfer function of a system is to cancel undesirable poles and zeroes of the system and substitute new poles and zeroes which are more favorable to the desired performance. These are restrictions on the concept of canceling zeroes with poles and poles with zeroes[3]. To study the forbidden cancellations, let it be assumed that the plant pulse transfer function contains one pole and one zero which lie outside the

[1, 2] Superscripts refer to reference numbers in Bibliography

unit circle in the Z plane. All the other singularities are assumed to lie inside the unit circle. Thus G(z) can be expressed by

$$G(z) = \frac{z - a_a}{z - b_a} F_g(z) \tag{3-1}$$

where a_a and b_a are the actual zero and pole of G(z), respectively, which lie outside the unit circle.

If the specified over-all pulse transfer function for this system is $K_s(z)$, then since

$$K_s(z) = \frac{D(z)G(z)}{1 + D(z)G(z)} \tag{3-2}$$

for unity feedback

$$D(z) = \frac{1}{G(z)}\left[\frac{K_s(z)}{1-K_s(z)}\right] \tag{3-3}$$

Substituting (3-1) into (3-3) but using a_d, b_d, and F_d desired values, instead of a_a, b_a, and F_a, actual values, there results

$$K_a(z) = \frac{(z-b_a)(z-a_a)F_g(z)K_s(z)}{(z-a_d)(z-b_a)[1-K_s(z)]F_d(z)+(z-b_d)(z-a_a)K_s(z)F_g(z)} \tag{3-4}$$

In the ideal situation, the poles and zeroes of the compensation cancel those of the plant exactly, so that

$$a_d = a_a$$

$$b_d = b_a$$

$$F_d(z) = F_a(z)$$

Then,
$$K_a(z) = K_s(z) \tag{3-6}$$

and the actual closed loop pulse transfer function is that which was specified.

In the practical situation however, exact cancellation of the plant poles and zeroes by the compensation poles and zeroes cannot be realistically expected, so that b_d and b_a or $a_d$and a_a are not exactly equal. This means that eqn. (3-4) cannot be reduced, and its poles and zeroes may lie outside the unit circle, as will be shown. To see this, let us assume that $F_d(z)$ and $F_a(z)$ are identical and that the imperfect cancellations are confined to poles and zeroes which lie outside the unit circle. Initially, it is assumed that the compensation zero and pole, a_d and b_d, are identical to the plant zero and pole, $a_a$and b_a, respectively. Under these conditions, perfect cancellation occurs, as has been shown. Now assume the plant zero and pole drift slightly by an amount Δa_a and Δb_a so these cancellations can no longer be made since the numerator and denominator of eqn. (3-4) differ.

The denominator of eqn. (3-4) is a polynomial in Z, and the locus of its roots as any parameter is varied, is continuous. Therefore, as the plant zero and pole, Δa_a and Δb_a shift slightly, the denominator roots shift slightly but are still outside the unit circle in the z plane, and they are not cancelled by equal roots in the numerator since the numerator roots shift in a different manner. Therefore, we should not attempt to cancel a pole outside the unit circle with a zero since a slight shift in either the plant or compensation results in instability.

In attempting to cancel a zero of eqn. (3-4)which is outside the unit circle with a pole requires the introduction of an unstable element in the compensation. In this case a slight shift again results in instability.

We require a restriction on the form of the specified pulse transfer function $K_s(z)$, so that cancellation of poles and zeroes of the plant pulse transfer function by the compensation pulse transfer function can be prevented. These restrictions are obtained by substituting the plant pulse transfer function from eqn. (3-1) into eqn. (3-3). Thus

$$D(z) = \frac{(z-b_a)}{(z-a_a)F_g(z)} \left[\frac{K_s(z)}{1-K_s(z)} \right] \qquad (3-7)$$

If $D(z)$ is not to contain a pole, a_a, and a zero, b_a, these terms must be contained in $K_s(z)$ and $1-K_s(z)$ respectively. Thus, in specifying a $K_s(z)$ which leads to a stable system, the following relations must be satisfied:

$$K_s(z) = (1-a_a z^{-1})\, M(z) \qquad (3-8)$$

$$1-K_s(z) = (1-b_a z^{-1}) N(z) \qquad (3-9)$$

where $M(z)$ and $N(z)$ are unspecified ratios of polynomials in z^{-1}. Stated in words:

> It is necessary that the specified over-all pulse transfer function $K_s(z)$ contain as its zeroes all those zeroes of the plant pulse transfer function which lie outside or on the unit circle in the z

plane - and that $1-K_s(z)$ contain as its zeroes all those poles of the plant pulse transfer function which lie outside or on the unit circle in the z plane.

Another requirement is that the response of the over-all system, $K_s(z)$, and the response of all system elements, D(z) and G(z), must be physically realizable. Taking G(z) first, we have in general, that

$$G(z) = \frac{P_m Z^{-m} + \ldots + P_n Z^{-n}}{q_o + q_1 Z^{-1} + \ldots q_b Z^{-b}} \qquad (3\text{-}10)$$

The presence of q_o in G(z) when it is expressed as the ratio of polynomials in Z^{-1} assures us that G(z) is physically realizable. This is shown readily by expanding G(z) into increasing powers of Z^{-1} as follows:

$$G(z) = aZ^{-m} + bZ^{-(m+1)} + \ldots \qquad (3\text{-}11)$$

where a, b, etc., are constants which are functions of the various p's and q's. Since G(z) defines the impulsive response of the plant, it follows that the presence of Z^{-m} as the first term assures the fact that the output of the plant does not preceed the input. In the limiting condition, the exponent m can be zero, although in practical plants it is never less than unity.

The transfer function D(z) has the same form as G(z) and is subject to the same restrictions.

$$D(Z) = \frac{a_o + a_1 Z^{-1} + \ldots + a_k Z^{-k}}{1 + b_1 Z^{-1} + b_2 Z^{-2} + \ldots b_j Z^{-j}} \qquad (3\text{-}12)$$

The restrictions on the overall transfer function, K(Z), may be found by substituting G(Z) and D(Z) into the expression for K(Z), i.e.

$$K(Z) = \frac{D(Z)\,G(Z)}{1 + D(Z)\,G(Z)} \qquad (3\text{-}13)$$

$$= \frac{\left[\frac{a_o + a_1 Z^{-1} + \ldots a_k Z^{-k}}{1 + b_1 Z^{-1} + b_2 Z^{-2} + \ldots + b_j Z^{-j}}\right]\left[\frac{P_m Z^{-m} + \ldots + P_n Z^{-n}}{q_o + q_1 Z^{-1} \ldots + q_b Z^{-b}}\right]}{1 + \left[\frac{a_o + a_1 Z^{-1} + \ldots a_k Z^{-k}}{1 + b_1 Z^{-1} + b_2 Z^{-2} + \ldots + b_j Z^{-j}}\right]\left[\frac{P_m Z^{-m} + \ldots + P_n Z^{-n}}{q_o + q_1 Z^{-1} + \ldots + q_b Z^{-b}}\right]}$$

Simplifying this expression and collecting terms, there results:

$$K(Z) = \frac{k_m Z^{-m} + \ldots + k_p Z^{-p}}{l_o + l_1 Z^{-1} + \ldots + l_q Z^{-q}} \qquad (3\text{-}14)$$

where the various k's and l's are combinations of the various p's, q's, a's, and b's.

It is concluded from this simple development that:

> in order to accomodate physically realizable elements in the closed loop, the numerator of the over-all pulse transfer function K(Z) must contain Z^{-1} to a power equal to and possibly greater than the lowest power m in the plant

pulse transfer function G(Z). Also it is necessary that the term 1_o appear in the denominator of K(Z) as shown in eqn. (3-14).

By observing these simple rules it is assured that the specified prototype does not require physically unrealizable components.

Another desirable system characteristic is that the output be properly related to the input in a finite amount of time. A general form for the overall transfer function is

$$K(Z) = \frac{C(Z)}{R(Z)} = \frac{\sum_{k=0}^{n-1} a_k Z^{-k}}{1 + \sum_{j=1}^{m-1} b_j Z^{-j}} \qquad (3\text{-}15)$$

$$\left[\sum_{k=0}^{n-1} a_k Z^{-k} \right] \left[1 + \sum_{j=1}^{m-1} b_j Z^{-j} \right]^{-1}$$

which can be written

$$C(Z) = \left[\sum_{k=0}^{n-1} a_k Z^{-k} \right] \left\{ 1 - \sum_{j=1}^{m-1} b_j Z^{-j} + \ldots + \left(\sum_{j=1}^{m-1} b_j Z^{-j} \right)^n + \ldots \right\} R(Z) \qquad (3\text{-}16)$$

where $n \to \infty$. In general, this is a non-terminating infinite series where the output is not properly related to the input in a finite amount of time.

An exception occurs when the input contains the quantity

$$1 + \sum_{j=1}^{m-1} b_j Z^{-j}$$

as a factor, but we will not be concerned with this case.

Inspection of eqn. (3-16) indicates that

an overall pulse transfer function, will possess

a finite settling time provided K(Z) is restricted

to a numerator polynomial in powers of Z^{-1}.

In a system utilizing sampled rather than continuous data, it is possible for the output to be in correspondence with the input at the sampling instants but to deviate between the sampling instants. This is termed output ripple. Thus far, we have not insured against the possibility of output ripple between the sampling instants. Further, we desire to eliminate the ripple from the plant while using a sample and hold digital-to-analog converter. Consequently if the system is to be ripple-free, the analog plant itself must be capable of generating the desired output from a constant (the output of the sample and hold). In the present case, the highest polynomial input is a ramp and the presence of an integrator (the motor) in the analog plant assures us of this capability.

The design problem then reduces to determining the error sequence transform $E_2(Z)/E_1(Z)$ (Fig. (1-1)) which will drive the system to this steady state condition after a transient period of fi-

nite length. The transform of the output number sequence $E_2(nT)$ that is applied to the hold unit is given by

$$E_2(Z) = \frac{C(Z)}{G(Z)}$$

but $$C(Z) = K(Z)\, R(Z)$$

therefore $$\frac{E_2(Z)}{R(Z)} = \frac{K(Z)}{G(Z)} \qquad (3\text{-}17)$$

To satisfy eqn (3-17) we need a constant relationship between $E_2(Z)$ and $R(Z)$ after a finite amount of time. Therefore, from what has been said before, we require the ratio of $E_2(Z)/R(Z)$ to be only a numerator polynomial in Z^{-1}. Eqn. (3-17) allows this condition to be contained in the specification of $K(Z)$. Alternatively then, we desire the ratio $K(Z)/G(Z)$ to be a numerator polynomial in Z^{-1}. Since $G(Z)$ is normally the ratio of two polynomials in Z^{-1}

$$G(Z) = \frac{N(Z)}{D(Z)} \qquad (3\text{-}18)$$

and $$\frac{K(Z)}{G(Z)} = \frac{K(Z)\ D(Z)}{N(Z)} \qquad (3\text{-}19)$$

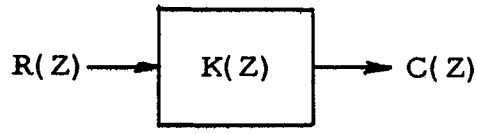
it is evident that $K(Z)$ must contain all the zeroes of $G(Z)$. This condition automatically includes the lesser condition that $K(Z)$ must contain those zeroes of $G(Z)$ that lie outside the unit circle.

To obtain a ripple free response, it is necessary that the analog portion of the

system be capable of generating a smooth polynomial from a set of discrete points, and that the over-all pulse transfer function, K(Z), must contain as its zeroes, all the zeroes of the plant transfer function, G(Z).

The output of our system can be ripple-free but still lag a ramp input. Now we require that our system achieve a no-error steady-state response to a ramp input.

For a system:



the error can be written

$$\epsilon = R(Z) - C(Z)$$

$$= R(Z) - R(Z)K(Z)$$

$$= R(Z)\left[\,1-K(Z)\right] \qquad (3\text{-}20)$$

For an input ramp

$$R(Z) = \frac{TZ^{-1}}{(1-Z^{-1})^2} \qquad (3\text{-}21)$$

$$\therefore \epsilon \text{ ramp} = \frac{TZ^{-1}}{(1-Z^{-1})^2}\left[\;1 - K(Z)\;\right] \qquad (3\text{-}22)$$

The Final Value Theorem states, that if f(t) is Laplace transformable and if the Laplace transform is F(s) then

$$\lim_{t\to\infty} f(t) = \lim_{n\to\infty} f[nT] - \lim_{Z^{-1}\to 1}(1-Z^{-1})\;F[Z]$$

Therefore, the steady-state ramp error is

$$\epsilon_{s\text{-}s_{ramp}} = \lim_{Z^{-1}\to 1} (1-Z^{-1}) \left\{ \frac{TZ^{-1}}{(1-Z^{-1})^2} \left[1 - K(Z) \right] \right\} \qquad (3\text{-}23)$$

Inspection of eqn. (3-23) indicates that:

> if the steady state ramp error is to be zero
> then $\left[1-K(Z) \right]$ must contain as a factor at least
> a term $(1-Z^{-1})^2$.

Even when all of the system characteristics enumerated thus far have been achieved, the response may not be considered "optimum". Usually, the designer also desires an "adequate" transient response. The transient response can be inferred using the methods of Nyquist, Bode, Nichols, Evans, etc. However, no general rules exist for specifying the optimum location of poles and zeroes.

Wiener has developed an elegant technique which accounts for noisy input signals. The result is an explicit mathematical statement of the desired system, expressed in terms of the signal and noise power spectra. Wiener's criteria is concerned with achieving the desired response in the presence of noise.

If our objective is to reproduce the input signal perfectly at the output of our system in the presence of noise, and we succeed, then the noise is also reproduced perfectly at the output. The total

output is thus perfect signal plus perfect noise. For a given system Wiener says there is a compensation which does not reproduce the signal perfectly, and therefore, neither does it reproduce the noise perfectly. However, Wiener's output which is the sum of the incorrect signal and incorrect noise is found to be closer to the correct signal than is the correct signal plus the correct noise. He obtains the compensation by knowing the statistical properties of both the noise and signal.

When the system use is general, we do not know the environment in which it will be used. However, we can design to minimize the effects of white noise. Random noise whose power density spectrum is flat over a band of frequencies which is considerably wider than the bandwidth of the system is termed white noise. The term "white" is taken from the term "white light" in optics.

Here, we desire to develop a criteria to minimize the effects of white noise at the input of our finite-settling-time system. We shall appeal to simple probability concepts.

Our system transfer function, K(Z), is restricted to being a numerator polynomial in Z^{-1} to possess a finite settling time. In discrete time, the output can be written:

$$c[nT] = \sum_{k=0}^{N-1} a_k r[(n-k)T] \qquad (3-24)$$

The Wiener criterion seeks to minimize the mean squared error. This results in choosing a set of a_i to minimize the mean squared output of the block diagram of Fig. 3-1. The input to the system is assumed to be a signal r(t) plus noise N(t). Hence the system output is

$$c\left[nT\right] = \sum_{k=0}^{N-1} a_k \left\{ r\left[(n-k)T\right] + N\left[(n-k)T\right] \right\} \quad (3\text{-}25)$$

To accomplish a compensation synthesis we need to specify some ideal process that acts on r(t) alone, producing a desired result $c_d(t)$, that is

$$r(t)\ I = c_d(t) \quad (3\text{-}26)$$

We define the error to be the difference between the actual and desired outputs

$$e\left[nT\right] = \sum_{k=0}^{N-1} a_k \left\{ r\left[(n-k)T\right] + N\left[(n-k)T\right] \right\} - c_d(t) \quad (3\text{-}27)$$

We may define the mean-squared error to be the time average:

$$\overline{e^2\left[nT\right]} = \lim_{M\to\infty} \frac{1}{M+1} \sum_{n=0}^{M} e^2\left[nT\right]$$

$$= \lim_{M\to\infty} \frac{1}{M+1} \sum_{n=0}^{M} \left[\sum_{k=0}^{N-1} a_k \left\{ r\left[(n-k)T\right] + N\left[(n-k)T\right] \right\} - c_d(t) \right]^2$$

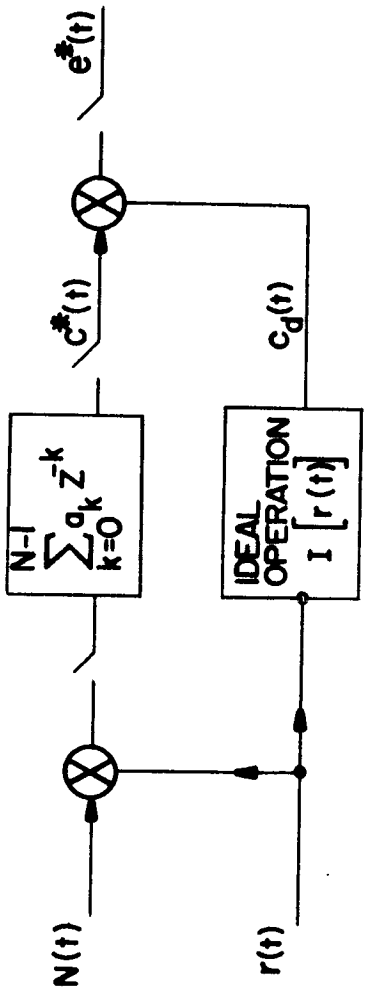


FIGURE 3-1 WIENER CRITERION FORMULATION

$$= \lim_{M\to\infty} \frac{1}{M+1} \sum_{n=0}^{M} \left\{ \sum_{k=0}^{N-1} \sum_{j=0}^{N-1} a_k a_j \, r\left[(n-k)T\right] r\left[(n-j)T\right] \right.$$

$$+C_d^2\left[nT\right] - 2C_d\left[nT\right] \sum_{k=0}^{N-1} a_k \, r\left[(n-k)T\right] + \sum_{k=0}^{N-1} \sum_{j=0}^{N-1} a_k a_j \, N\left[(n-k)T\right] N\left[(n-j)T\right]$$

$$+ \sum_{k=0}^{N-1} \sum_{j=0}^{N-1} a_k a_j \, r\left[(n-k)T\right] N\left[(n-j)T\right] - 2C_d\left[nT\right] \sum_{k=0}^{N-1} a_k N\left[(n-k)T\right]$$

$$\left. + \sum_{k=0}^{N-1} \sum_{j=0}^{N-1} a_j a_k \, N\left[(n-j)T\right] \, r\left[(n-k)T\right] \right\} \qquad (3\text{-}28)$$

Now, it is convenient to introduce the notion of the discrete equivalent of an autocorrelation and cross correlation function. Let us define these to be:

$$\psi_{xx}\left[kT\right] = \lim_{M\to\infty} \frac{1}{M+1} \sum_{n=0}^{M} X\left[nT\right] X\left[(n-k)T\right] \qquad (3\text{-}29)$$

$$\psi_{xy}\left[kT\right] = \lim_{M\to\infty} \frac{1}{M+1} \sum_{n=0}^{M} Y\left[nT\right] X\left[(n-k)T\right] \qquad (3\text{-}30)$$

$$\psi_{yx}\left[kT\right] = \lim_{M\to\infty} \frac{1}{M+1} \sum_{n=0}^{M} X\left[nT\right] Y\left[(n-k)T\right] \qquad (3\text{-}31)$$

Then making these substitutions we may write eqn. 3-28 as

$$\overline{e^2\, nT} = \left\{ \sum_{k=0}^{N-1} \sum_{j=0}^{N-1} a_k a_j \, \psi_{rr}\left[(k-j)T\right] + \overline{C_d^2\left[nT\right]} - 2 \sum_{k=0}^{N-1} a_k \psi_{rc_d}\left[kT\right] \right\}$$

$$+ \sum_{k=0}^{N-1} \sum_{j=0}^{N-1} a_k a_j \psi_{NN}\left[(k-j)T\right] + \sum_{k=0}^{N-1} \sum_{j=0}^{N-1} a_k a_j \psi_{rN}\left[(k-j)T\right]$$

$$-2 \sum_{k-0}^{N-1} a_k \psi_{NC_d}\left[kT\right] + \sum_{k=0}^{N-1} \sum_{j=0}^{N-1} a_k a_j \psi_{N_r}\left[(k-j)t\right] \qquad (3\text{-}32)$$

The first three terms within the braces are referred to as the systematic error, for they contribute to the mean-squared error only if the system fails to perform the ideal operation. The last four terms arise because of the input noise N(t). These terms are the random source of error. The last three terms are nonzero only if the noise and the signal are correlated.

If we assume that the systematic error is zero and the signal and noise are uncorrelated, as is true with white noise, then

$$\overline{e^2[nT]} = \sum_{k=0}^{N-1} \sum_{j=0}^{N-1} a_k a_j \psi_{NN}\left[(k-j)T\right] \qquad (3\text{-}33)$$

Noise that is correlated for less than one sampling interval T implies that $\psi_{NN}\left[(k-j)T\right]$ is nonzero only for k=j. It follows directly from the definition of correlation that

$$\psi_{NN}\left[(k-j)T\right]_{k=j} = \psi_{NN}\left[0\right] = \psi_{NN}$$

$$= \text{mean squared value of the noise}$$
$$= \text{constant} \qquad (3\text{-}34)$$

We refer to noise that has this property as "almost white". Clearly, any noise can appear almost white to a digital computer.

We only have to select a sufficiently large T.

For almost white noise, eqn. (2-33), becomes

$$\overline{e^2[nT]} = \sigma_N^2 \sum_{k=0}^{N-1} a_k^2$$

and

$$\frac{\overline{e^2[nT]}}{\sigma_N^2} = \sum_{k=0}^{N-1} a_k^2 \qquad (3\text{-}35)$$

This ratio is called the variance reduction factor and is a measure of the "almost white" noise reduction properties of the system.

To minimize the effects of white noise present at the input, we desire to minimize the factor $\sum_{k=0}^{N-1} a_k^2$ where the individual a_k are the coefficients of the overall transfer function k(Z). It is desired that this factor be less than unity.

Reduction of the Systematic Error

In the expression (eqn 3-28) for the mean squared error, we referred to the first three terms as the systematic error. These terms are zero when the system performs the ideal operation.

These three terms (re-arranged) are:

$$\sum_{k=0}^{N-1} \sum_{j=0}^{N-1} a_k a_j \, r[(n-k)T] \, r[(n-j)T] - 2C_d[nT] \sum_{k=0}^{N-1} a_k \, r[(n-k)T] + C_d^2[nT] = 0 \qquad (3\text{-}36)$$

Which can be written

$$\left[\sum_{k=0}^{N-1} a_k r\left[(n-k)T\right] - C_d\left[nT\right] \right]^2 = 0 \tag{3-37}$$

and this requires that

$$C_d\left[nT\right] = \sum_{k=0}^{N-1} a_k r\left[(n-k)T\right] \tag{3-38}$$

To see for what class of inputs, $r\left[(n-k)T\right]$, the above equation can be true, let us introduce the first backward difference function of $f[x]$ [4], i.e.

$$\nabla f\,[x] \triangleq f[x] - f[x-1] \tag{3-39}$$

The second backward difference, denoted by $\nabla^2 f[x]$ is the first difference of $\nabla f[x]$, i.e.

$$\begin{aligned} \nabla^2 f[x] = \nabla(\nabla f[x]) &= \nabla f[x] - \nabla f[x-1] \\ &= f[x] - 2f[x-1] + f[x-2] \end{aligned} \tag{3-40}$$

and, in general,

$$\nabla^n f[x] = \nabla(\nabla^{n-1} f[x]) \tag{3-41}$$

Another useful operator is the backward shift operator defined by

$$E^{-1} f[x] = f[x-1] \tag{3-42}$$

If we define

$$E^{-2} f[x] = E^{-1}(E^{-1} f[x])$$

Then it follows that

$$E^{-2} f[x] = f[x-2] \tag{3-43}$$

and, in general

$$E^{-n}f[x] = f[x-n] \tag{3-44}$$

Now, let us write eqn 3-40 using this notation,

$$\nabla^2 f[x] = (1-2E^{-1} + E^{-2})\, f[x]$$

$$= (1-E^{-1})^2 f[x]$$

From the definitions of E^{-1} and ∇ it necessarily follows that

$$\nabla = (1-E^{-1})$$

from which

$$E^{-1} = 1-\nabla \tag{3-45}$$

The conditions which will eliminate the systematic error (eqn 3-38) can be written

$$C_d[nT] = \sum_{k=0}^{N-1} a_k E^{-k} r[nT] = \sum_{k=0}^{N-1} a_k (1-\nabla)^k r[nT]$$

$$= \sum_{k=0}^{N-1} a_k \left\{ 1 - \binom{k}{1}\nabla + \binom{k}{2}\nabla^2 + \ldots + (-1)^k \nabla^k \right\} r[nT] \tag{3-46}$$

Therefore, to eliminate the systematic error, the desired output $C_d[T]$ must be a function that is expressible in terms of a backward difference of not higher than the k^{th} order. Therefore, a polynomial input of degree equal to or less than N-1, is one for which the systematic error can be reduced to zero.

In this system, the inputs are, a step function and a ramp, so the systematic error can be reduced to zero. However, there is a basic difficulty. Later, it will be seen that there is a unit delay in the memory drum and also a unit delay in the

sample and hold circuitry. To minimize the effects of these two delays, let us require that the digital compensation predict forward an amount (αT), where α is any real number, in general, or 2 in this case.

$$\therefore C_d[nT] = r[(n+\alpha)T] = \sum_{k=0}^{N-1} a_k r[(n-k)T] \qquad (3\text{-}47)$$

If we consider the response to a polynomial of degree of $q \leq (N-1)$. Then

$$r[nT] = a_o + a_1[nT] + a_2[nT]^2 + \ldots + a_q[nT]^q \qquad (3\text{-}48)$$

$$r[(n+\alpha)T] = a_o + a_1[(n+\alpha)T] + a_2[(n+\alpha)T]^2 + \ldots + a_q[(n+\alpha)T]^q \qquad (3\text{-}49)$$

and $$r[(n-k)T] = a_o + a_1[(n-k)T] + a_2[(n-k)T]^2 + \ldots + a_q[(n-k)T]^q \qquad (3\text{-}50)$$

Now, if we define the differential operator D

$$D^i x[t] \triangleq \frac{d^i x}{dt^i} \qquad (3\text{-}51)$$

then we may write an expression for a differentiable function $x[t]$ about a point $t = \alpha$ by means of a Taylor series:

$$x[t] = x[\alpha] + D[\alpha](t-\alpha) + D^2[\alpha]\left(t-\frac{\alpha}{2}\right)^2 + \ldots D^i[\alpha]\frac{(t-\alpha)^i}{i!} \qquad (3\text{-}52)$$

Now, we may identify

$$\alpha = nT$$

$$t = (n+k)T \qquad (3\text{-}53)$$

then

$$x\left[(n+k)T\right] = x\left[nT\right] + Dx\left[nT\right]\frac{kT}{1!} + D^2x\left[nT\right]\frac{(kT)^2}{2!} + \ldots + D^ix\left[nT\right]\frac{(kT)^i}{i!}$$

$$= \sum_{i=0}^{\infty} \frac{(kT)^i}{i!} D^i x\left[nT\right] \qquad (3\text{-}54)$$

Eqn(3-47) can be written:

$$\sum_{i=0}^{\infty} \frac{(\alpha T)^i}{i!} D^i r\left[nT\right] = \sum_{k=0}^{N-1} a_k \sum_{i=0}^{q} \frac{(-kT)^i}{i!} D^i r\left[nT\right] \qquad (3\text{-}55)$$

but

$$\sum_{i=0}^{\infty} \frac{(\alpha T)^i}{i!} D^i r\left[nT\right] = \sum_{i=0}^{q} \frac{(\alpha T)^i}{i!} D^i r\left[nT\right] + \sum_{i=q+1}^{\infty} \frac{(\alpha T)}{i!} D^i r\left[nT\right]$$

and for a finite polynomial of degree q the last term is zero.

Hence eqn (3-55) can be written

$$\sum_{i=0}^{q} \left\{ \alpha^i - \sum_{k=0}^{N-1} a_k (-k)^i \right\} \left(\frac{T^i D^i}{i!} \right) r\left[nT\right] = 0 \qquad (3\text{-}56)$$

Since the braced expression must hold for every i up to and including i = q, the necessary and sufficient conditions for this equation to be satisfied are

$$\sum_{k=0}^{N-1} a_k = 1 \qquad i=0$$

$$\sum_{k=0}^{N-1} k a_k = -\alpha \qquad i=1$$

$$\sum_{k=0}^{N-1} k^2 a_k = \alpha^2 \qquad i = 2 \qquad (3\text{-}57)$$

$$\vdots$$

$$\sum_{k=0}^{N-1} k^q a_k = (-1)^q a^q \qquad i=q$$

for polynomials of order $q \leq (n-1)$.

Thus from the Wiener expression for the mean squared error, our servo compensation requirement can now be stated thus: We desire to follow an input signal which can be expressed by a polynomial of degree q, also, we desire to minimize the effects of white noise at the input, and further, due to the necessary delays in the drum and sample and hold circuitry, we desire to predict ahead two units of time so there is no following error.

This can be accomplished by minimizing eqn (3-35) subject to the set of constraints (3-57).

To determine the coefficients a_k of eqn (3-24) subject to the set of constraints (3-57) and simultaneously to minimize the variance reduction factor (3-35), we can utilize the principle of Lagrangian multipliers.[5]

To minimize a function

$$f\left[a_k\right] = \sum_{k=0}^{N-1} a_k^2 \qquad (3\text{-}35)$$

subject to a set of constraints (3-57), one forms an auxiliary function

$$f\left[a_k; \lambda_i\right] = \sum_{k=0}^{N-1} a_k^2 + 2\lambda_o \left\{ \sum_{k=0}^{N-1} a_k - 1 \right\} + 2\lambda_1 \left\{ \sum_{k=0}^{N-1} k a_k + a \right\} + \ldots 2\lambda_q \left\{ \sum_{k=0}^{N-1} k^q a_k - (-a)^q \right\} \qquad (3\text{-}58)$$

where the $2\lambda_i$ are known as Lagrangian multipliers. The principle to be used here, is that, in order for the original function $f[a_k]$ to reach a minimum under the set of constraints (3-57) it is a necessary condition that the derivative of $f[a_k; \lambda_i]$ with respect to the a_k also reach a minimum.

Summary of Compensation Design Criteria

Before proceeding with the detailed compensation design, it seems advisable to list the conditions which our over-all system must satisfy in order to: be ripple free, provide no steady-state error to a step and/or ramp function, and to minimize the effects of white-noise at the input.

1. It is necessary that the specified overall pulse transfer function $K_s(Z)$ contain as its zeroes all those zeroes of the plant pulse transfer function which lie outside or on the unit circle in the Z-plane, and, that $1-K_s(Z)$ contain as its zeroes all those poles of the plant pulse transfer function which lie outside or on the unit circle in the Z-plane.

2. In order to accommodate physically realizable elements in the closed loop, the numerator of the overall pulse transfer function K(Z) must contain Z^{-1} to a power equal to or possibly greater than the lowest power m in the

plant pulse transfer function G(Z). Also, it is necessary that the term l_o appear in the denominator of K(Z) as shown in eqn. (3-14) K(Z), G(Z), and D(Z) must all be physically realizable and have the same form.

3. In order to possess a finite settling time, the overall pulse transfer function K(Z) is restricted to a numerator polynomial in powers of Z^{-1}.

4. To obtain a ripple free response, it is necessary that the analog portion of the system be capable of generating a smooth polynomial from a set of discrete points, and that the overall pulse transfer function, K(Z) must contain as its zeroes, all the zeroes of the plant transfer function G(Z). Notice, that this condition is stronger than condition 1.

5. To respond to a ramp input with zero steady-state error $\left[1-K(Z)\right]$ must contain as a factor at least a term $(1-Z^{-1})^2$.

6. To minimize the effects of white noise present at the input, we desire to minimize the variance reduction factor $\sum_{k=0}^{N-1} a_k^2$

7. To achieve an ideal response, i.e. a systematic error of zero, with a unit time delay in the memory and a

unit time delay in the memory and a unit time delay in the sample and hold circuitry, we must utilize prediction and satsify eqn. set (3-57) for $a = 2$.

Conditions 6 and 7 are simultaneously satisfied when the auxiliary function $f[a_k, \lambda_i]$ given in eqn. (3-58) is minimized.

When condition 6 is satisfied for a ramp input, condition 5 is satisfied. Condition 1 is satisfied when condition 4 is satisfied.

The compensation design problem reduces to satisfying conditions 2, 3, 4, and eqn (3-58). Condition 2 is satisfied on the basis of form and our result will be shown to be physically realizable. Conditions 3, 4, and eqn set (3-57) can be combined into a new eqn set.

Recall from eqn (2-20) the transfer function of our plant, that the plant contains two zeroes.

Conditions 2 and 3 are satisfied by an overall transfer function of the following form:

$$K(Z) = \sum_{k=0}^{N-1} a_k Z^{-(k+m)} \qquad (3\text{-}59)$$

To satisfy condition 4

$$K(Z) = (1+bZ^{-1})(1+cZ^{-1}) \sum_{k=0}^{N-1} \beta_k Z^{-(k+m)} \qquad (3\text{-}60)$$

where in this design

$$b = 1.4811$$

and $$c = 0.0451$$

Equating eqns. (3-59) and (3-60)

$$\sum_{k=0}^{N-1} a_k Z^{-(k+m)} = \left[1+(b+c)Z^{-1}+bcZ^{-2}\right] \sum_{k=0}^{N-1} \beta_k Z^{-(k+m)}$$

$$= \beta_o Z^{-m} + \beta_o (b+c) Z^{-(m+1)} + \beta_o bc Z^{-(m+2)}$$

$$+ \beta_1 \quad Z^{-(m+1)} + \beta_1 (b+c) Z^{-(m+2)} + \beta_1 bc Z^{-(m+3)}$$

$$+ \beta_2 \quad Z^{-(m+2)} + \beta_2 (b+c) Z^{-(m+3)} + \beta_2 bc Z^{-(m+4)} + \ldots$$

$$= \beta_o Z^{-m} + \left[\beta_1+\beta_o(b+c)\right] Z^{-(m+1)} + \left[\beta_2+\beta_1(b+c)+\beta_o(bc)\right] Z^{-(m+2)}$$

$$+ \left[\beta_3+\beta_2(b+c)+\beta_1(bc)\right] Z^{-(m+3)} + \ldots \qquad (3\text{-}61)$$

The variance reduction factor (eqn. 3-35) can now be written:

$$\sum_{k=0}^{N-1} a_k^2 = \beta_o^2 + \left[\beta_1+\beta_o(b+c)\right]^2 + \left[\beta_2+\beta_1(b+c)+\beta_o(bc)\right]^2 + \ldots \qquad (3\text{-}62)$$

Also, from eqn. (3-61) we can write:

$$\sum_{k=0}^{N-1} a_k = \beta_o + \left[\beta_1+\beta_o(b+c)\right] + \left[\beta_2+\beta_1(b+c)+\beta_o bc\right] + \ldots$$

$$= \left[1 + (b+c) + bc\right] \sum_{k=0}^{N-1} \beta_k \qquad (3\text{-}63)$$

In eqn. set (3-57) we require a term $\sum_{k=0}^{N-1} k a_k$. Using eqn. (3-61)

$\sum_{k=0}^{N-1} k a_k$	=	
$0.\, a_1$	=	$0 : \beta_o$
$1.\, a_2$	=	$1\left[\beta_1 + \beta_o(b+c)\right]$
$2.\, a_2$	=	$2\left[\beta_2 + \beta_1(b+c) + \beta_o bc\right]$
$3.\, a_3$	=	$3\left[\beta_3 + \beta_2(b+c) + \beta_1 bc\right]$
.	.	.
.	.	.
.	.	.
$(N-1)a_{N-1}$	=	$(N-1)\left[\beta_{N-1} + \beta_{N-2}(b+c) + \beta_{N-3} bc\right]$

(3-64)

The right side of eqn. (3-64) can be written

$$\sum_{k=0}^{N-1} k a_k = \sum_{k=0}^{N-1} k\beta_k + \sum_{k=0}^{N-1} (k+1)(b+c)\beta_k + \sum_{k=0}^{N-1} (k+2)bc\,\beta_k$$

$$= \sum_{k=0}^{N-1} k\,\beta_k + (b+c)\sum_{k=0}^{N-1} k\beta_k + bc\sum_{k=0}^{N-1} k\beta_k + (b+c)\sum_{k=0}^{N-1} \beta_k + (bc)\sum_{k=0}^{N-1} \beta_k$$

$$= \left[1+(b+c) + bc\right]\sum_{k=0}^{N-1} k\beta_k + \left[(b+c) + bc\right]\sum_{k=0}^{N-1} \beta_k \qquad (3\text{-}65)$$

Under condition 7 we must satisfy eqn. set (3-57). For a ramp input we need satisfy only the first two equations of the set. These are

$$\sum_{k=0}^{N-1} a_k = 1$$

$$\sum_{k=0}^{N-1} k a_k = -\alpha \tag{3-66}$$

From eqns. (3-63) and (3-66)

$$\sum_{k=0}^{N-1} a_k = 1 = \left[1+(b+c)+bc\right] \sum_{k=0}^{N-1} \beta_k$$

$$\therefore \sum_{k=0}^{N-1} \beta_k = \frac{1}{1 + (b+c) + bc} \tag{3-67}$$

From eqns. (3-65) and (3-66)

$$\sum_{k=0}^{N-1} k a_k = -\alpha = \left[1 + (b+c) + bc\right] \sum_{k=0}^{N-1} k\beta_k + \left[(b+c) + bc\right] \sum_{k=0}^{N-1} \beta_k \tag{3-68}$$

Using eqn. (3-67)

$$-\alpha = \left[1+ (b+c) + bc\right] \sum_{k=0}^{N-1} k\beta_k + \frac{(b+c) + bc}{1+ (b+c) + bc}$$

$$\therefore \sum_{k=0}^{N-1} k\beta_k = -\left\{ \frac{\alpha \left[1 + (b+c) + bc\right] + \left[(b+c) + bc\right]}{\left[1 + (b+c) + bc\right]^2} \right\} \tag{3-69}$$

Condition 7 is now satisfied by eqns. (3-67) and (3-68)

Now, to obtain equations for condition 6, let us rewrite eqn. (3-58) to the extent required for a ramp.

$$f[a_k; \lambda_i] = \sum_{k=0}^{N-1} a_k^2 - 2\lambda_o \left\{ \sum_{k=0}^{N-1} a_k - 1 \right\} - 2\lambda_1 \left\{ \sum_{k=0}^{N-1} k a_k + \alpha \right\} \tag{3-70}$$

Substituting eqns (3-62), (3-63) and (3-65) into (3-70) we may write

$$f\left[\beta_k;\lambda_i\right] = \beta_o^2 + \left[\beta_1+\beta_o\,(b+c)\right]^2 + \left[\beta_2 + \beta_1(b+c) + \beta_o(bc)\right]^2 + \ldots$$
$$-2\lambda_o\left\{\left[1 + (b+c) + bc\right]\sum_{k=0}^{N-1}\beta_k - 1\right\}$$
$$-2\lambda_1\left\{\left[1 + (b+c) + bc\right]\sum_{k=0}^{N-1} k\beta_k + \left[(b+c)+ bc\right]\sum_{k=0}^{N-1}\beta_k + a\right\} \qquad (3\text{-}71)$$

To minimize eqn.(3-70), we can minimize eqn. (3-71) by setting its partial derivatives to zero, i. e.,

$$\frac{\partial f\left[\beta_x,\ \lambda_i\right]}{\partial f\ \beta_k} = 0 \qquad (3\text{-}72)$$

and obtain a new equation set:

$$\frac{\partial f}{\partial\beta_o} = 2\beta_o + 2\left[\beta_1+\beta_o\,(b+c)\right](b+c) + 2\left[\beta_2+\beta_1(b+c)+\beta_o(bc)\right]bc$$
$$- 2\lambda_o\left[1 + (b+c) + bc\right] - 2\lambda_1\left[(b+c) + bc\right] = 0$$

$$\frac{\partial f}{\partial\beta_1} = 2\left[\beta_1+\beta_o\,(b+c)\right] + 2\left[\beta_2+\beta_1(b+c)+\beta_o bc\right](b+c) + 2\left[\beta_3+\beta_2\,(b+c)+\beta_1 bc\right]bc$$
$$-2\lambda_o\left[1+(b+c)+bc\right] - 2\lambda_1\left\{\left[1+(b+c)+bc\right] + \left[(b+c)+bc\right]\right\} = 0$$

$$\frac{\partial f}{\partial\beta_2} = 2\left[\beta_2+\beta_1(b+c)+\beta_o bc\right] + 2\left[\beta_3+\beta_2(b+c)+\beta_1 bc\right](b+c) + 2\left[\beta_4+\beta_3(b+c)+\beta_2 bc\right]bc$$
$$-2\lambda_o\left[1+(b+c)+bc\right] - 2\lambda_1\left\{2\left[1+(b+c)+bc\right] + \left[(b+c)+bc\right]\right\} = 0$$
$$\vdots$$
$$\vdots \qquad (3\text{-}73)$$

$$\frac{\partial f}{\partial\beta_{N-3}} = 2\left[\beta_{N-3}+\beta_{N-4}(b+c)+\beta_{N-5}bc\right] + 2\left[\beta_{N-2}+\beta_{N-3}(b+c)+\beta_{N-4}bc\right](b+c)$$
$$+2\left[\beta_{N-1}+\beta_{N-2}(b+c)+\beta_{N-3}bc\right]bc - 2\lambda_o\left[1+(b+c)+bc\right] - 2\lambda_1\left\{(N-3)\left[1+(b+c)+bc\right]\right.$$
$$\left. + \left[(b+c)+bc\right]\right\} = 0$$

Eqn. set (3-73) plus eqns., (3-67) and (3-69) are the complete design equations. These equations are given in matrix form in Fig (3-2). The numerical values for our design case, b = 1.4811 and c=0.0451 are shown also for the case where K = 5.

To obtain the coefficients which satisfy the matrix, the program shown in Fig (3-3) was used in a Univac 1107. The computer time required to solve the matrix was 5 seconds. The answers are listed in Fig (3-2).

To determine the expression for the compensation, D(Z), we use the solution of the matrix given in Fig (3-2) and eqn. (3-60) which is repeated here for convenience.

$$k(Z)= (1+bZ^{-1})\ (1+cZ^{-1}) \sum_{k=0}^{N-1} \beta_k Z^{-(k+m)} \qquad (3\text{-}60)$$

where

b = 1.4811
c = 0.0451
m = 2

$$K(Z) = (1+1.4811Z^{-1})\ (1+0.0451Z^{-1}) \Big[0.396635Z^{-2} + 0.319192Z^{-3} + -0.281014Z^{-4} + 0.439475Z^{-5} - 0.356271Z^{-6} \ -0.132349Z^{-7} \Big] \qquad (3\text{-}74)$$

Recalling that there is a unit delay associated with the use of the drum and using eqn. (3-3) we obtain

$$Z^{-1}D(Z) = \frac{K(Z)}{G(Z)\left[1-K(Z)\right]} \qquad (3\text{-}75)$$

but condition 5 of the compensation design criteria required that $\left[1-K(Z)\right]$ contain a factor $(1-Z^{-1})^2$. Therefore, we can factor a $(1-Z^{-1})$ and using eqn. (3-61) obtain

$$
\begin{bmatrix}
-\left[1+(b+c)+bc\right] & -\left[(b+c)+bc\right] & 1+(b+c)^2+(bc)^2 & (b+c)(1+bc) & bc & 0 & \cdots & 0 \\
-\left[1+(b+c)+bc\right] & -\left[1+2\ (b+c)+bc\right] & (b+c)(1+bc) & 1+(b+c)^2+(bc)^2 & (b+c)(1+bc) & bc & \cdots & 0 \\
-\left[1+(b+c)+bc\right] & -\left[2+3\ (b+c)+bc\right] & bc & (b+c)(1+bc) & 1+(b+c)^2+(bc)^2 & (b+c)(1+bc) & \cdots & 0 \\
-\left[1+(b+c)+bc\right] & -\left[3+4\ (b+c)+bc\right] & 0 & bc & (b+c)(1+bc) & 1+(b+c)^2+(bc)^2 & \cdots & 0 \\
\vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \cdots & 0 \\
\vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \cdots & bc \\
\vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \cdots & (b+c)(1+bc) \\
-\left[1+(b+c)+bc\right] & -\left[(N-3)+(N-2)\left[(b+c)+bc\right]\right] & 0 & 0 & 0 & bc & (b+c)(1+bc) & 1+(b+c)^2+(bc)^2 \\
\hline
0 & 0 & 1 & 1 & 1 & 1 & \cdots & 1 \\
0 & 0 & 0 & 1 & 2 & 3 & \cdots & N-2 \quad N-1
\end{bmatrix}
\begin{bmatrix} \lambda_0 \\ \lambda_1 \\ \beta_0 \\ \beta_1 \\ \vdots \\ \beta_{n-2} \\ \beta_{n-1} \end{bmatrix}
=
\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ \vdots \\ 0 \\ \dfrac{1}{1+(b+c)+bc} \\ -\left\{\dfrac{a\left[1+(b+c)+bc\right]+\left[(b+c)+bc\right]}{\left[1+(b+c)+bc\right]^2}\right\} \end{bmatrix}
$$

$$
\begin{bmatrix}
-2.592998 & -1.592998 & 2.329734 & 1.526883 & 0.066798 & 0 & 0 & 0 \\
-2.592998 & -4.185994 & 1.526883 & 2.329734 & 1.526883 & 0.066798 & 0 & 0 \\
-2.592998 & -6.778994 & 0.066798 & 1.526883 & 2.329734 & 1.526883 & 0.066798 & 0 \\
-2.592998 & -9.371992 & 0 & 0.066798 & 1.526883 & 2.329734 & 1.526883 & 0.066798 \\
-2.592998 & -11.964990 & 0 & 0 & 0.066798 & 1.526883 & 2.329734 & 1.526883 \\
-2.592998 & -14.557988 & 0 & 0 & 0 & 0.066798 & 1.526883 & 2.329734 \\
\hline
0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 \\
0 & 0 & 0 & 1 & 2 & 3 & 4 & 5
\end{bmatrix}
\begin{bmatrix} \lambda_0 \\ \lambda_i \\ \beta_0 \\ \beta_1 \\ \beta_2 \\ \beta_3 \\ \beta_4 \\ \beta_5 \end{bmatrix}
=
\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0.385668 \\ -1.011241 \end{bmatrix}
$$

Answers:

$\lambda_0 = 0.642068$
$\lambda_1 = -0.170892$
$\beta_0 = 0.396635$
$\beta_1 = 0.319192$
$\beta_2 = -0.281014$
$\beta_3 = 0.439475$
$\beta_4 = -0.356271$
$\beta_5 = -0.132349$

FIGURE 3-2 SYSTEM COEFFICIENT MATRIX

IV IMPLEMENTATION OF THE DIGITAL COMPENSATION

From the form of the compensation equation 3-78we can see that addition, subtraction, and the multiplication of delayed quantities by a coefficient are some of the basic operations required in the digital compensator. It will be shown that the basic integrator building block of a Digital Differential Analyzer (DDA) is useful in the compensator. Due to the incremental form of solution the DDA possesses a natural solution-time advantage over a General Purpose (GP) digital computer for continuous control processes[6].

The DDA integrator[7] utilizes the geometric analogy shown in Fig. (4-1) and is organized as shown in Fig (4-2). The fundamental integrator equations are:

$$y[nT] = y[(n-1)T] + \Delta y[nT] \qquad (4\text{-}1)$$

$$\Delta Z[nT] + R[nT] = y[nT]\Delta x[nT] + R[(n-1)T] \qquad (4\text{-}2)$$

That is to say:

The present ordinate equals the past ordinate

plus the change in the ordinate.

and,

The present integrator output, plus the present remainder equals the present ordinate times the present change in the abscissa plus the past remainder.

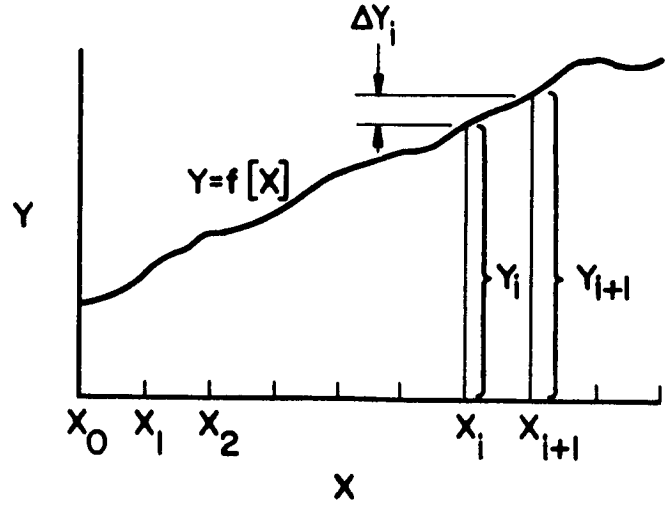


FIGURE 4-1 GEOMETRIC ANALOGY OF DIGITAL INTEGRATOR

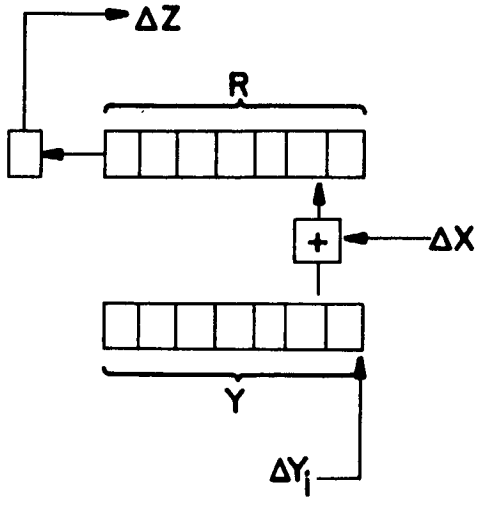


FIGURE 4-2 DDA ORGANIZATION OF DIGITAL INTEGRATOR

When $\Delta x = \Delta t = 1$ unit, the integration is accomplished by merely adding $y[nT]$ to $R[(n-1)T]$ once each computer cycle. In the DDA integrator manufactured by Computer Controls Corporation[8] one line is used for ΔZ and the output can have two values +1 and -1. In the DDA integrator manufactured by Bendix Corp., two lines are used for ΔZ (one for sign, the other for magnitude) and the output can have three values +1, 0, and -1. When the ΔZ of integrator (j) is unity each cycle and becomes the Δy of integrator (k), the maximum rate of rise of integrator (k) occurs. On a normalized basis, this maximum rate of rise is one unit of ordinate per one unit of time or a 45^{o} rise.

Thus, while the arithmetic unit of this integrator type is simple, the frequency response is limited accordingly. When used in a DDA computer to solve, say, differential equations, the computer can be programmed to run in non-real time and the effective frequency response improved. Also, in this type of application, accuracy can be increased at the expense of a longer solution time.

However, when a DDA integrator is used to compensate a plant, it must operate in real time and it is very desirable for it to possess a high frequency response. (maximum slope approaching 90^{o}) and yet to maintain a fine resolution. This can be seen with the aid of Fig. (4-3). Assume the accumulated

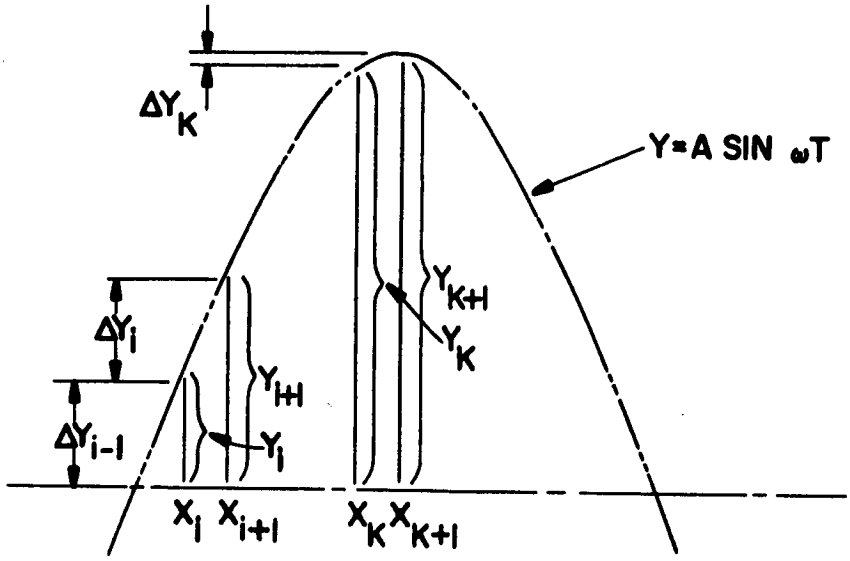


FIGURE 4-3 RANGE OF ΔY FOR FREQUENCY RESPONSE & ACCURACY

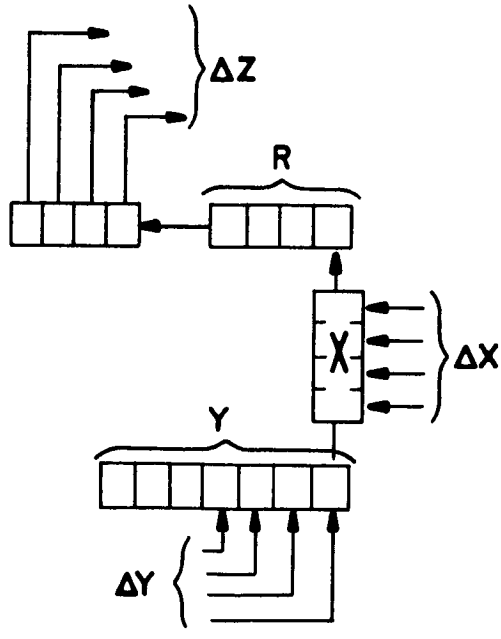


FIGURE 4-4 MULTIPLE INCREMENT INTEGRATOR

```
COMMENT GAUSSIAN REDUCTION FOR N EQUATIONS IN N UNKNOWNS M179 NM 1 2
        R) W) REARNS      FOR INVERSION AND SOLUTION USE  IS 1
        FOR INVERSION USE IS 2 FOR SOLUTION USE IS 3  R ROWS  C COL $
INTEGER USE, R, C, I, J, L, H, T, U, V, Y $
        ARRAY A(20,40), CNT(20), SOL(20) $
LA1.. READ($$ ROWS) $ READ($$ COLUMNS) $ READ($$ PURPOSE) $
      READ($$ MATRIX) $ READ($$ CONSTANT) $
INPUT ROWS(R), COLUMNS(C), PURPOSE(USE),
      MATRIX  ( FOR I = (1,1,R) $ FOR J = (1,1,C) $ A(I,J)),
      CONSTANT ( FOR L = (1,1,R) $ CNT(L)) $
FOR Y = (1,1, (R - 1)) $
        BEGIN DIV = A(Y,Y) $
              IF DIV EQL 0 $ BEGIN WRITE ($$PIVOTHEAD) $
                             WRITE ($$ZEROPIVOT, FORM3) $
                               OUTPUT ZEROPIVOT(Y) $
                             GO TO LA5 $ END $
              FOR J = (Y+1,C) $ A(Y,J) = (A(Y,J))/(DIV) $
              FOR U = ((Y + 1), 1,R) $
                   BEGIN T = Y $ MULT = -(A(U,T)) $
                   FOR V = (Y,1,C)$ A(U,V) = A(U,V) + (MULT)(A(Y,V))$
                   END $
        END $
DIV = A(R,R) $ FOR J = (R,1,C) $ A(R,J) = A(R,J)/(DIV) $
FOR Y = (R, -1, 2) $
        BEGIN FOR I = ((Y - 1), -1, 1) $
                   BEGIN MULT = -(A(I,Y)) $
         FOR H = (Y,1,C) $ A(I,H) = A(I,H) + (MULT)(A(Y,H)) $
                   END $
        END $
IF USE EQL 3 $ GO TO LA3 $
LA5.. WRITE($$ INVERSE, FORM1) $
        OUTPUT INVERSE( FOR I = (1,1,R) $ FOR J = (1,1,C) $ A(I,J)) $
        FORMAT FORM1(6S10.6, W2), FORM2(B15, S10.6, W4),
              PIVOTHEAD(B10,*PIVOT COEFF YY IS ZERO  Y IS BELOW*,
              W4), FORM3(B22, I3, W0) $
IF USE EQL 2 $ GO TO LA4 $
LA3.. FOR I = (1,1,R) $
        BEGIN FOR J = (1,1,R) $
             SOL(I) = SOL(I) + (CNT(J))(A(I,(R + J))) $
        END $
WRITE($$ SOLUTION, FORM2) $
        OUTPUT SOLUTION( FOR I = (1,1,R) $ SOL(I))$
LA4.. FINISH $
COMPLETE
```

FIGURE 3-3 UNIVAC 1107 BALGOL PROGRAM

$$[1-k(Z)] = (1-Z^{-1})\,[1+Z^{-1}+0.603365Z^{-2}-0.321171Z^{-3}-0.553802Z^{-4}$$
$$-0.585714Z^{-5}-0.881399Z^{-6}-0.234665Z^{-7}-0.008876Z^{-8}] \qquad (3\text{-}76)$$

Using the expression for G(Z) given in eqn. (2-20) and substituting into eqn. (3-62), we obtain

$$Z^{-1}D(Z) = \frac{(1+1.4811Z^{-1})(1+0.0451Z^{-1})Z^{-2}[0.396635+0.319192Z^{-1}}{\dfrac{0.00229Z^{-1}(1+1.4811Z^{-1})(1+0.0451Z^{-1})(1+Z^{-1})}{(1-Z^{-1})(1-0.67Z^{-1})(1-0.0025Z^{-1})}\left[1+Z^{-1}\right.}$$
$$\left.-\frac{-0.281014Z^{-2}+0.439475Z^{-3}-0.356271Z^{-4}-0.132349Z^{-5}}{+0.603365Z^{-2}-0.321171Z^{-3}-0.553802Z^{-4}}\right.$$
$$\left.-0.585714Z^{-5}-0.881399Z^{-6}-0.234665Z^{-7}-0.132349Z^{-8}\right. \qquad (3\text{-}77)$$

The digital compensation required is

$$D(Z) = \frac{1.25\,(0.317080+0.041964Z^{-1}-0.396006Z^{-2}+0.503194Z^{-3}-0.521831Z^{-4}}{1+Z^{-1}+0.603365Z^{-2}-0.321171Z^{-3}-0.553802Z^{-4}-0.585714Z^{-5}}$$
$$\frac{+0.086393Z^{-5}+0.070726Z^{-6}-0.000177Z^{-7}}{-0.881399Z^{-6}-0.234665Z^{-7}-0.132349Z^{-8}} \qquad (3\text{-}78)$$

The response of the compensated plant is available from

$$c(Z) = R(Z)\,K(Z) \qquad (3\text{-}79)$$

For a step function input

$$R_s(Z) = \frac{1}{1-Z^{-1}} \qquad (3\text{-}80)$$

The corresponding response is given in Fig 3-4 (a)

For a ramp function input

$$R_r(Z) = \frac{Z^{-1}}{(1-Z^{-1})^2} \tag{3-81}$$

The corresponding response is given in Fig (3-4) (b).

The output response is continuous but calculated output values are plotted only at the sample times.

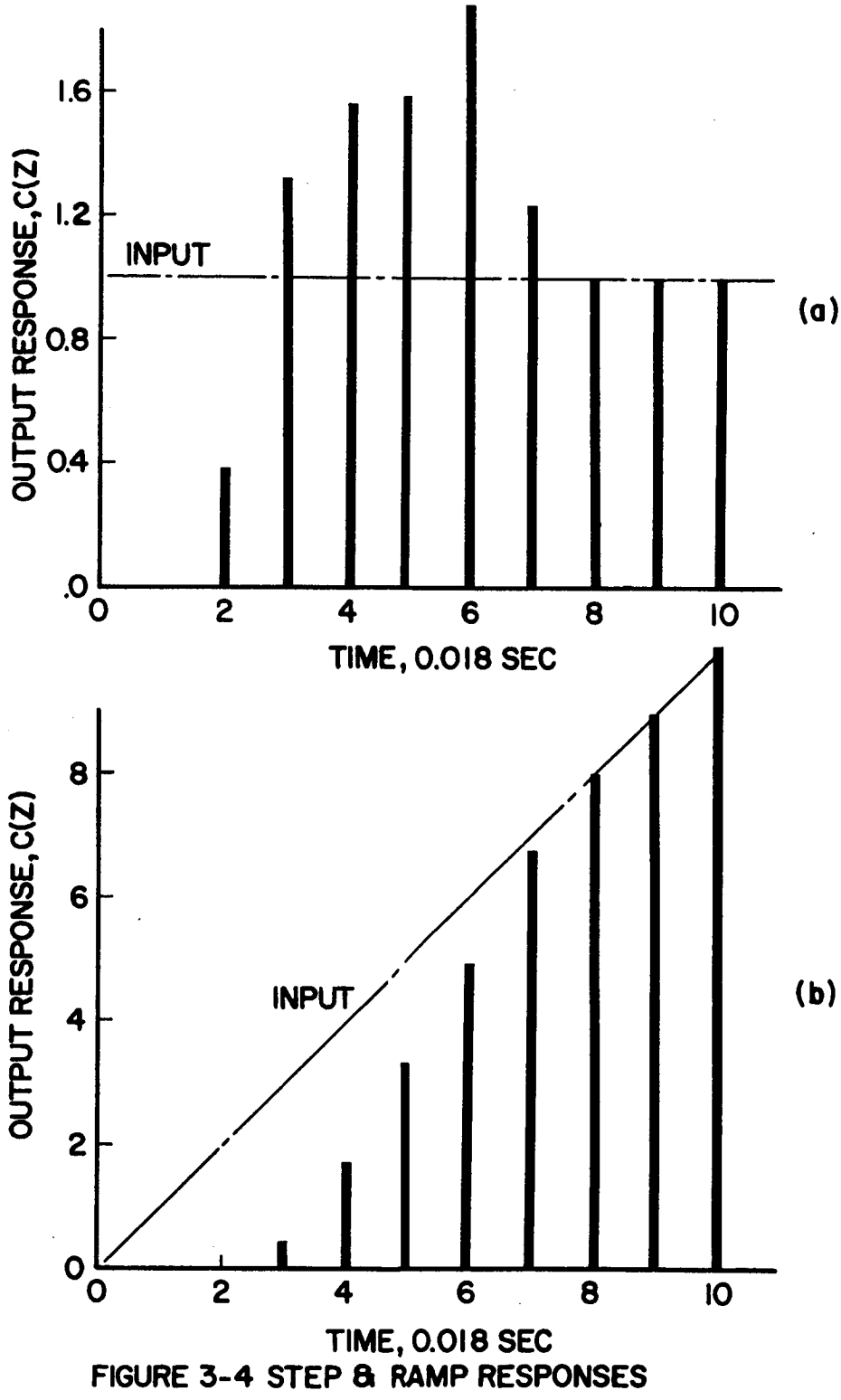


FIGURE 3-4 STEP & RAMP RESPONSES

output from an integrator should approximate a continuous sine wave of frequency ω. Where the sine-wave crosses the abscissa we require a large output from the integrator per unit time, while near the peak of the wave, we require a small output.

Truncation errors arise due to the form of series approximation chosen to represent the integral. As in the calculus, it is only when we pass to the limit that we obtain a correct solution. In the DDA integrator, we do not pass to the limit but utilize a finite ΔX. To reduce the truncation error, when necessary, various forms of interpolation schemes are used.

Round off errors arise due to the use of finite registers and not carrying an infinite number of binary places. Also, when the output of one integrator is the input to a second, the second y register is short by the amount remaining in the remainder register of the first integrator. This can be seen by re-arranging eqn. (3-2).

$$\Delta Z[nT] = y[nT]\Delta x[nT] + R[(n-1)T] - R[nT] \qquad (4-3)$$

and using eqn. (2-39)

$$\Delta Z[nT] = y[nT]\Delta x[nT] - \Delta R[nT] \qquad (4-4)$$

What is desired then is to make the first term as large as possible to gain frequency response and to minimize the second term to improve accuracy.

This is the basis for the multiple increment integrator

shown in Fig 4-4. The remainder is reduced by extending multiple lines to the right. When multiple lines are provided to the left, the capacity of the integrator is increased. Multiple lines are also shown for Δx, since the integrator is not restricted to integrating with respect to time.

To show how the multiple increment technique enters the scaling, we can first write the equations for $\Delta Z = +1$, 0, or -1 operation.

The scaling of the problem limits the value of $y[nT]$

$$-1 \leq y[nT] \leq +1 \tag{4-5}$$

also $$y[nT]\Delta x[nT] \leq \epsilon \tag{4-6}$$

If we half fill the R register (to represent zero), the problem of $\pm$ R is avoided because R will always be positive.

$$0 \leq R[(n-1)T] \leq \epsilon \tag{4-7}$$

From eqn. (4-6)

$$-\epsilon \leq y[nT]\Delta x[nT] \leq \epsilon$$

and $$-\epsilon \leq y[nT]\Delta x[nT] + R[(n-1)T] \leq 2\epsilon$$

Eqn. (3-7) is also true for $R[nT]$

We obtain a single output from eqn (3-2) when

$$\frac{\Delta Z}{\epsilon} = \text{integral part of} \left[\frac{y[nT]\Delta x[nT] + R[(n-1)T]}{\epsilon} \right] \tag{4-8}$$

Now

$$\Delta Z = \begin{cases} -\epsilon & \text{when } -\epsilon \leq y[nT]\Delta x[nT] + R[(n-1)T] < 0 \\ 0 & \text{when } 0 \leq y[nT]\Delta x[nT] + R[(n-1)T] < \epsilon \\ +\epsilon & \text{when } \epsilon \leq y[nT]\Delta x[nT] + R[(n-1)T] < 2\epsilon \end{cases} \tag{4-9}$$

In the multiple increment integrator, if we being n lines around (two to the left, the rest to the right of the binary point)

$$0 \leq R\left[(n-1)T\right] < \frac{\epsilon}{2^{n-2}} \qquad (4\text{-}10)$$

$$y\left[nT\right]\Delta x\left[nT\right] \leq 2\epsilon$$

$$-2\epsilon \leq y\left[nT\right]\Delta x\left[nT\right] \leq 2\epsilon \qquad (4\text{-}11)$$

If n=1 we obtain 2 values -1, +1

n=2 we obtain 3 values -1, 0, +1

n=3 we obtain 7 values -1.5, -1.0, -0.5, 0, +0.5, +1.0, +1.5

. . .

. . .

. . .

n=n we obtain 2^{n-1} values.

Eqn. (4-11) contains the term 2ϵ because in the limit $\Delta x\left[nT\right]$ can equal 2ϵ.

Therefore by providing additional multiple lines to the right of the binary point, then the maximum rate of change is increased by 2 and the minimum resolution is $\epsilon / 2^{n-2}$.

Fig 4-4 shows that in the multiple increment DDA integrator, when ΔZ extends to the right of the binary point, the maximum remainder is reduced leading to more accurate integration. If the multiple increment ΔZ extends to the left of the binary point the maximum rate of rise (frequency response) of the integrator is increased.

A DDA can integrate with respect to a variable other than time. When the variable Δx is unit time, the addition of

$y[nT]$ to $R[(n-1)T]$ suffices. But if Δx is the output of another integrator with multiple increments, y must first be multiplied by a multiple increment Δx and then added to R. Thus, the arithmetic unit of a multiple increment integrator must perform multiplication while the arithmetic unit of a single increment DDA integrator need perform only addition.

Note that when the ordinate y is a constant, which will be shown to be true in the present case, the rectangular integration rule is perfectly accurate and no truncation error exists. Thus the multiple increment technique is capable of minimizing the source of integration error.

To see what role a DDA integrator can play in implimenting our digital compensation let us inspect the performance of three integrators in series as shown in Fig 4-5. In this arrangement the ordinates are constants and the output of integrator n becomes the Δx of integrator n-1.

Applying eqn (3-2) to integrator n, we obtain,

$$\Delta x_o[nT] + R_o[nT] = a_o \Delta x[nT] + R_o[(n-1)T]$$

$$\Delta x_o[nT] = a_o \Delta x[nT] + R_o[(n-1)T] - R_o[nT]$$

$$= a_o \Delta x[nT] - R_o[nT][1-Z^{-1}]$$

but $1-Z^{-1} = \Delta$

$$\therefore \Delta x_o\ nT = a_o \Delta x[nT] - \Delta R_o[nT] \qquad (4-12)$$

In a similar manner

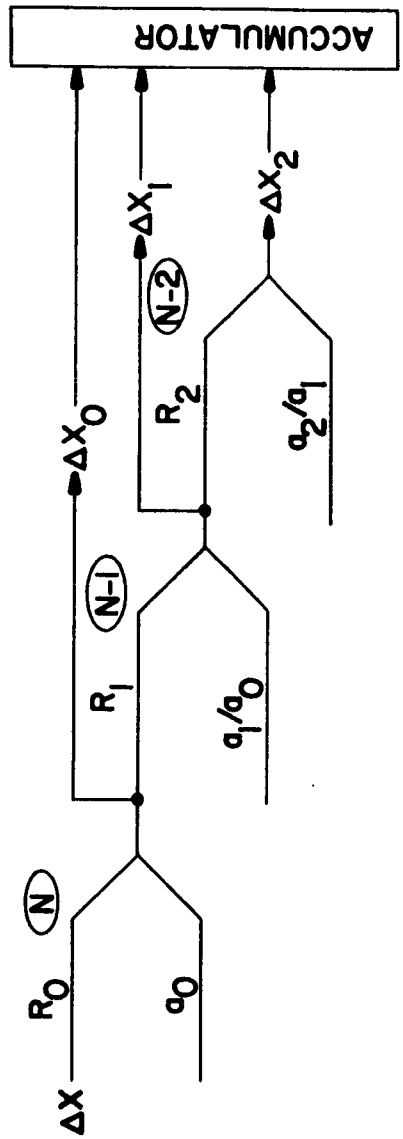


FIGURE 4-5 THREE DDA INTEGRATORS IN SERIES

$$\Delta x_1[nT] = \frac{a_1}{a_o}\Delta x_o[nT] - \Delta R_1[nT] \qquad (4\text{-}13)$$

and $$\Delta x_2[nT] = \frac{a_2}{a_1}\Delta x_1[nT] - \Delta R_2[nT] \qquad (4\text{-}14)$$

Substituting eqn. (4-12) into eqn. (4-13), we obtain

$$\Delta x_1[nT] = \frac{a_1}{a_o}\left\{ a_o\Delta x[nT] - \Delta R_o[nT] \right\} - \Delta R_1[nT]$$

$$= \frac{a_1}{a_o}\, a_o\Delta x[nT] - \frac{a_1}{a_o}\Delta R_o[nT] - \Delta R_1[nT] \qquad (4\text{-}15)$$

and substituting eqn (4-15) into eqn (4-14) we obtain

$$\Delta x_2[nT] = \frac{a_2}{a_1}\left\{ \frac{a_1}{a_o}\, a_o\Delta x[nT] - \frac{a_1}{a_o}\Delta R_o[nT] - \Delta R_1[nT] \right\}$$

$$-\Delta R_2[nT] \qquad (4\text{-}16)$$

and,

$$\Delta x_2[nT] = \frac{a_2}{a_1}\,\frac{a_1}{a_o}\, a_o\,\Delta x[nT] - \frac{a_2}{a_1}\,\frac{a_1}{a_o}\Delta R_o[nT] - \frac{a_2}{a_1}\Delta R_1[nT] - \Delta R_2[nT] \qquad (4\text{-}17)$$

Now, if we sum the three outputs using eqns (4-12), (4-15), and (4-17) we obtain

$$(\Delta x_o + \Delta x_1 + \Delta x_2)[nT] = (a_o + a_1 + a_2)\,\Delta x - (1 + \frac{a_1}{a_o} + \frac{a_2}{a_o})\,\Delta R_o[nT]$$

$$- (1 + \frac{a_2}{a_1})\,\Delta R_1[nT] - \Delta R_2[nT]$$

$$= (a_o + a_1 + a_2)\,\Delta x - \frac{(a_o + a_1 + a_2)}{a_o}\,\Delta R_o[nT] -$$

$$\frac{-(a_1+a_2)\,\Delta R_1[nT] - \Delta R_2[nT]}{a_1} \qquad (4\text{-}18)$$

Let us see what occurs if we allow the integrators to overflow from left to right, and store the value of the overflow until the next time interval, while processing the integrators from right to left in sub-interval time sequence.[5]

At the beginning of the time interval $t = [(n-2)T]$ the stored overflows have the following values.

$$\begin{aligned} \Delta x_2[(n-2)T] &= 0 \\ \Delta x_1[(n-2)T] &= 0 \\ \Delta x_o[(n-2)T] &= 0 \\ \Delta x\,[(n-2)T] &= \text{the new incoming value} \end{aligned} \qquad (4\text{-}19)$$

$\Delta x_1[(n-2)T]$ is zero, therefore the output of integrator (n-2) which is stored as $\Delta x_2[(n-1)T]$, is zero. Similarly, the $\Delta x_o[(n-2)T]$ is zero, therefore the output of integrator (n-1) which is stored as $\Delta x_1[(n-1)T]$, is zero. Since $\Delta x[(n-2)T]$ has a value, using eqn (4-12) we obtain,

$$\Delta x_o[(n-1)T] = a_o\,\Delta x[(n-2)T] - \Delta R_o[(n-1)T] \qquad (4\text{-}20)$$

At the beginning of the time interval, $t = [(n-1)T]$, the stored overflows have the following values:

$$\begin{aligned} \Delta x_2[(n-1)T] &= 0 \\ \Delta x_1[(n-1)T] &= 0 \\ \Delta x_o[(n-1)T] &= \text{see eqn (4-20)} \\ \Delta x\,[(n-1)T] &= \text{the new incoming value} \end{aligned} \qquad (4\text{-}21)$$

$\Delta x_1 \left[(n-1)T \right]$ is zero, therefore the output of integrator (n-2) which is stored as $\Delta x_2(nT)$, is zero. $\Delta x_o \left[(n-1)T\right]$ has the value of eqn (4-21), therefore the output of integrator (n-1) which is stored as $\Delta x_1(nT)$ is

$$\Delta x_1 \left[nT\right] = \frac{a_1}{a_o} \; a_o \, \Delta x \left[(n-2)T\right] - \frac{a_1}{a_o} \; \Delta R_o \left[(n-1)T \right] - \Delta R_1 \left[nT \right] \tag{4-22}$$

and similarly

$$\Delta x_o \left[nT\right] = a_o \Delta x \left[(n-1)T\right] - \Delta R_o \left[nT\right] \tag{4-23}$$

At the beginning of the time interval, $t = \left[nT\right]$, the stored overflows have the following values

$$\begin{aligned} \Delta x_2 \left[nT\right] &= 0 \\ \Delta x_1 \left[nT\right] &= \text{see eqn (4-22)} \\ \Delta x_o \left[nT\right] &= \text{see eqn (4-23)} \\ \Delta x \left[nT\right] &= \text{the new incoming value} \end{aligned} \tag{4-24}$$

Since $\Delta x_1 \left[nT\right]$ has a value, the output of integrator (n-2) which is stored as $\Delta x_2 \left[(n-1)T\right]$ is

$$\Delta x_2 \left[(n+1)T\right] = \frac{a_2}{a_1} \cdot \frac{a_1}{a_o} \cdot a_o \, \Delta x \left[(n-2)T\right] - \frac{a_2}{a_1} \cdot \frac{a_1}{a_o} \Delta R_o \left[(n-1)T \right] - \frac{a_2}{a_1} \Delta R_1 \left[nT\right]$$

$$- \Delta R_2 \left[(n+1)T \right] \tag{4-25}$$

similarly,

$$\Delta x_1 \left[(n+1)T\right] = \frac{a_1}{a_o} \cdot \; a_o \; \Delta x \left[(n-1)T\right] - \frac{a_1}{a_o} \; \Delta R_o \left[nT\right] - \Delta R_1 \left[(n+1)T\right] \tag{4-26}$$

and

$$\Delta x_o \left[(n+1)T\right] = a_o \Delta x \left[nT\right] - \Delta R_o \left[(n+1)T\right] \tag{4-27}$$

TIME	ACCUMULATOR = $\Sigma \Delta x_i$
$t = [(n-2)T]$	$0 + 0 + a_o \Delta x[(n-2)T] - \Delta R_o[(n-1)T]$
$t = [(n-1)T]$	$0 + a_1 \Delta x[(n-1)T] + a_o \Delta x[(n-1)T] - a_1 \Delta R_o[(n-1)T] - (\Delta R_1 + \Delta R_2)[nT]$
$t = [(nT)]$	$a_2 \Delta x[(n-2)T] + a_1 \Delta x[(n-1)T] + a_o \Delta x[nT] - a_2 \Delta R_o[(n-1)T] - \left(\frac{a_2}{a_1} \Delta R_1 + \frac{a_1}{a_o} \Delta R_o\right)[nT] - (\Delta R_1 + \Delta R_o)[(n+1)T]$

(4-28)

Table 4-1 Accumulator contents vs time

Notice that the change in the remainder value of each integrator can be either plus or minus. Also, the coefficients may have different signs so that the accumulator error tends to be small. It will be shown that the new value for Δx is the actuating error for the system so that as Δx becomes small, the change in the remainders also become small.

If we assume, $\Delta R = 0$ and note that

$$\Delta x\left[(n-1)T\right] = Z^{-1}\,\Delta x\left[nT\right] \tag{4-29}$$

then at $t = \left[(nT)\right]$ the value in the accumulator is

$$\Sigma x_i = \Delta x\left[nT\right]\left(a_o + a_1 Z^{-1} + a_2 Z^{-2}\right) \tag{4-30}$$

Equation (4-30) is of the same form as the numerator portion of the required compensation (eqn 3-65).

The compensation given in eqn (3-78) is of the general form:

$$Z^{-1}D(Z) = Z^{-1}\,\frac{E_2(Z)}{E_1(Z)} = \frac{\sum_{k=0}^{N-1} a_k Z^{-k}}{1 - \sum_{l=1}^{M-1} b_l Z^{-l}}$$

or

$$E_2(Z)\left[1 - \sum_{l=0}^{M-1} b_l Z^{-l}\right] = E_1(Z)\sum_{k=0}^{N-1} a_k Z^{-k}$$

$$E_2\left[nT\right] = \sum_{k=0}^{N} a_k E_1\left[(n-k)T\right] . + \sum_{l=0}^{M} b_l E_2\left[(n-1)T\right] \tag{4-31}$$

That is, the present error at the sample and hold circuit, $E_2(nT)$ (see Fig 1), is a function of a finite number of past actuating errors, $E_1\left[(n-k)T\right]$, and a finite number of past digital compensator outputs, $E_2\left[(n-1)T\right]$.

The complete digital program for eqn 3-78 is given in Fig. (4-6). The integrators overflow from left to right while the individual integrators are processed in the sequence of the circled numbers.

Referring to Fig (4-6) again, we see that integrators 0 through 7 are processed in that order. The overflow from each integrator is summed in the Accumulator as shown. Note that the processing of these integrators is repetitious. During the time that an integrator number 8 could be processed, the actuating error of the servo is computed and becomes the source of the cascading overflows. These operations result in the center term of eqn (4-31). Integrator space 9 is left blank in accordance with the manner of handling overflows which will be explained later. Integrators 10 thru 17 are then processed, in that order, in an identical manner to 0 thru 7 except that the source of cascading overflows is the last accumulator value. These operations result in the third term of eqn (4-31). When all the overflows from integrators 0 thru 7 are summed with those from integrators 10 thru 17, the result is the present compensator output, which is the first term of eqn (4-31).

Essentially, then, we require 16 integrators (with repetitious processing), a means of computing the actuating error, an accumulator, and a means of processing the accumulator, and a means of processing the accumulator. The overflows must occur from left to right and the integrators must be processed in the order shown in Fig (4-6).

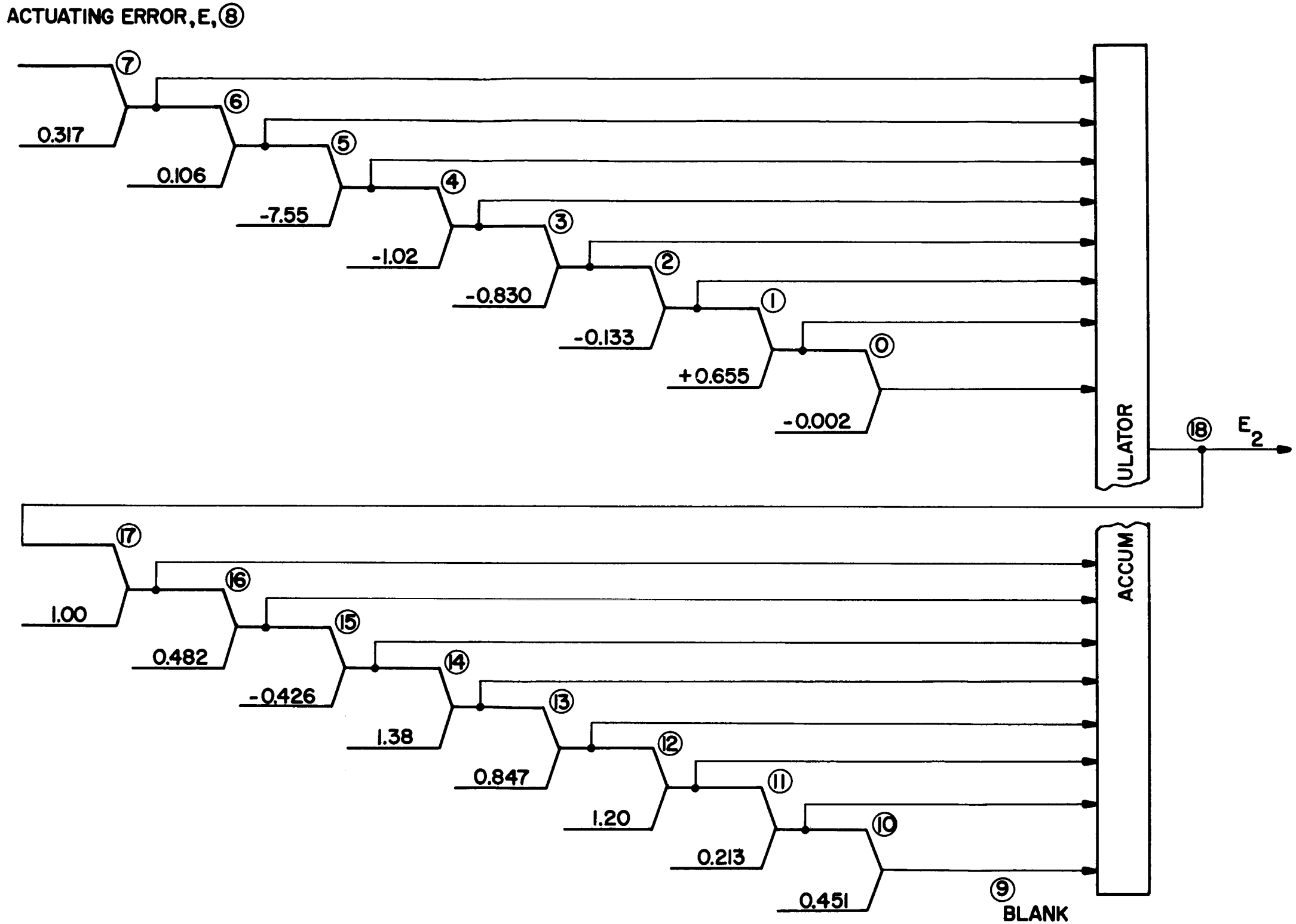


FIGURE 4-6 COMPENSATION FLOW DIAGRAM

From our discussion of our multiple increment integrator, we know that in processing each integrator we must:

1. Obtain the value of the constant corresponding to the integrator. y = constant.
2. Obtain the value of the overflow from the next integrator which occurred during the previous processing time. $\Delta Z_j\left[(n-1)T\right] = \Delta x_i\left[nT\right]$.
3. Obtain the value of the remainder left in the integrator during the previous processing time. $R_i\left[(n-1)T\right]$.

Then, in accordance with eqn (4-2) we must multiply $y\left[nT\right]$ by $\Delta x\left[nT\right]$ and add the product to the previous remainder to obtain the present overflow and new remainder. The present overflow must then be made available to the integrator just previously processed. The overflow must also be totaled in the accumulator.

Since this process must be repeated 16 times per cycle, we seek a method which is economical of equipment. Notice that one arithmetic unit can be time shared with all the integrators since they are processed sequentially. Then notice each integration requires three values at the start: a constant, a previous remainder, and an overflow. After processing there is obtained an overflow, and a new remainder. The constant can be discarded since it is the same for each integrator each cycle. These are merely storage requirements, where the new remainder replaces the old, and an overflow is placed in a lagging storage address.

A magnetic drum was selected for the storage unit. It is quite an economical means of storage. It's operation is sequential,

and the compensator is readily expandable merely by providing either a larger diameter or more storage spaces per circumferential inch. It will be shown later, that the compensator with the present 10-inch diameter drum is capable of compensating 10 servos simultaneously.

The drum surface is divided into sectors as shown in Fig 4-7. Each sector is sub-divided into 32 addresses. Thirty-two is merely a convenient number (2^5) and one which allows safety factors of space. The speed of the drum surface varies but on the average the addresses are separated in time by 12μsec. This spacing is compatable with the 100kc read-write rate of magnetic drums. In fact these units, although operating near their design limits, are establishing only a basic rate. Unique arithmetic circuitry, to be described later, was developed to perform the addition of 18-bit words between each 12μsec interval.

Although multiplication is described in Chapter V, it is necessary to mention here that multiplication is handled as repeated addition.

In order to give the reader an overall view of the compensator and to explain how the overflows pass between integrators a system block diagram is given in Fig (4-8). The basic integrator is shown in the center. The overflows from ΔZ are accumulated and also stored to become the source of Δx. Each cycle the accumulator total is transferred to the sample and hold unit from where the information is converted to A-C carrier

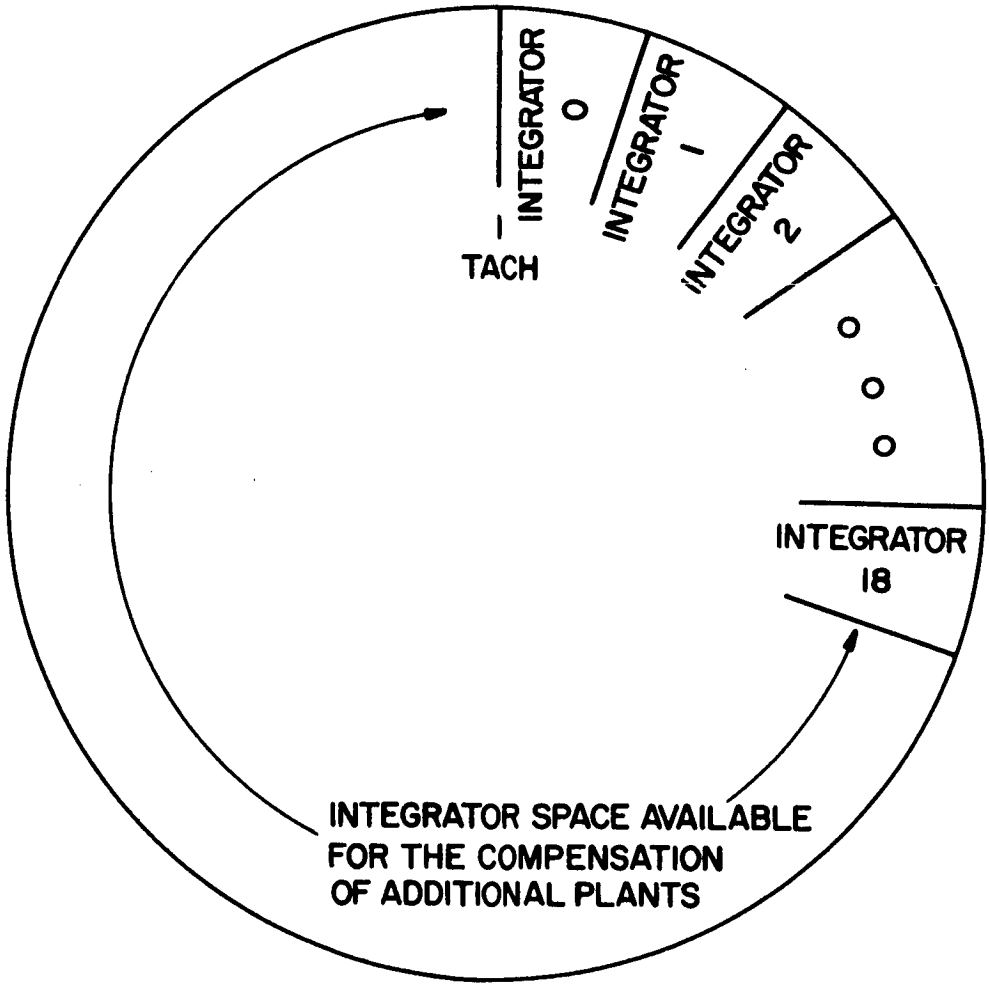


FIGURE 4-7 INTEGRATOR SPACING ON DRUM SURFACE

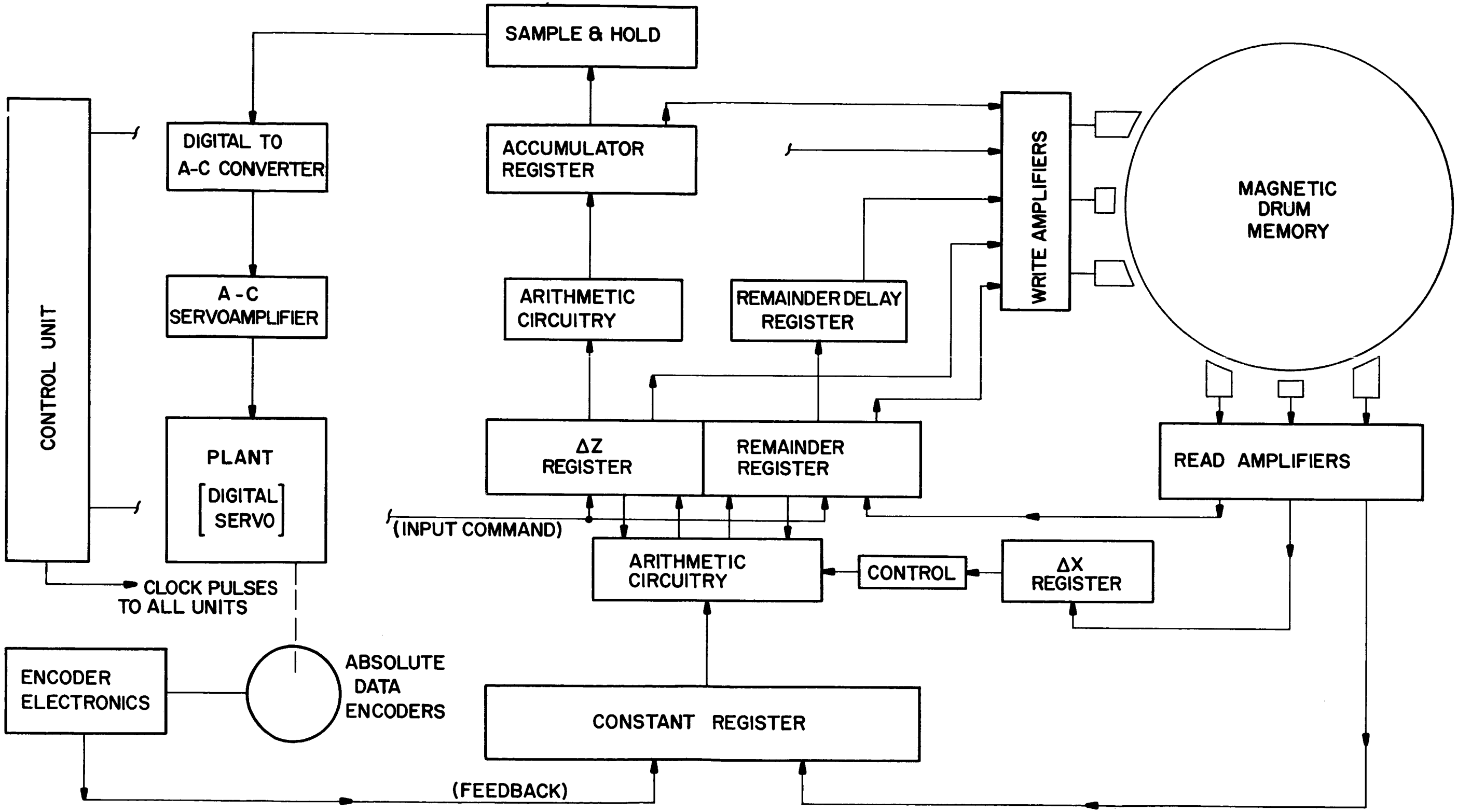


FIGURE 4-8 SYSTEM BLOCK DIAGRAM

form to drive the servomotor of the plant.

The remainder delay register assists in converting ΔZ overflows to Δx commands. This may be seen with the aid of Fig (4-9). It is suggested that the reader duplicate part (b) of the figure which represents a portion of the drum circumference. Part (a) represents the stationary read write heads and contains the remainder delay register.

Shift part (b) to the left so that the dotted lines are lined up at the START position. At this time the remainder delay register contains the remainder of the previous integrator (on the right). At T0, we read C. At T2, we read R. At T4, we read Δx. From this time to T23 the integrator is processed, as will be described later. At T24, we write the contents of the remainder delay register into position T4 of the previous integrator (on the right). The remainder is now written with its own integrator. At T26, we take the overflow (ΔZ) from the integrator on the left and write it as ΔX of the previous integrator. By by-passing any delay, the overflow is advanced on the drum surface. Also, during T26, we reset the remainder delay register. At T28, we transfer the remainder into the remainder delay register. In this manner, the overflows "walk" with respect to the drum surface. Because it takes two integrator periods to process an integrator, integrator 9 is left blank in Fig. (4-6) because the actuating error is formed during the time period of integrator 8.

Except for the details of the arithmetic operation, the reader can understand the first column of the clock timing diagram given in

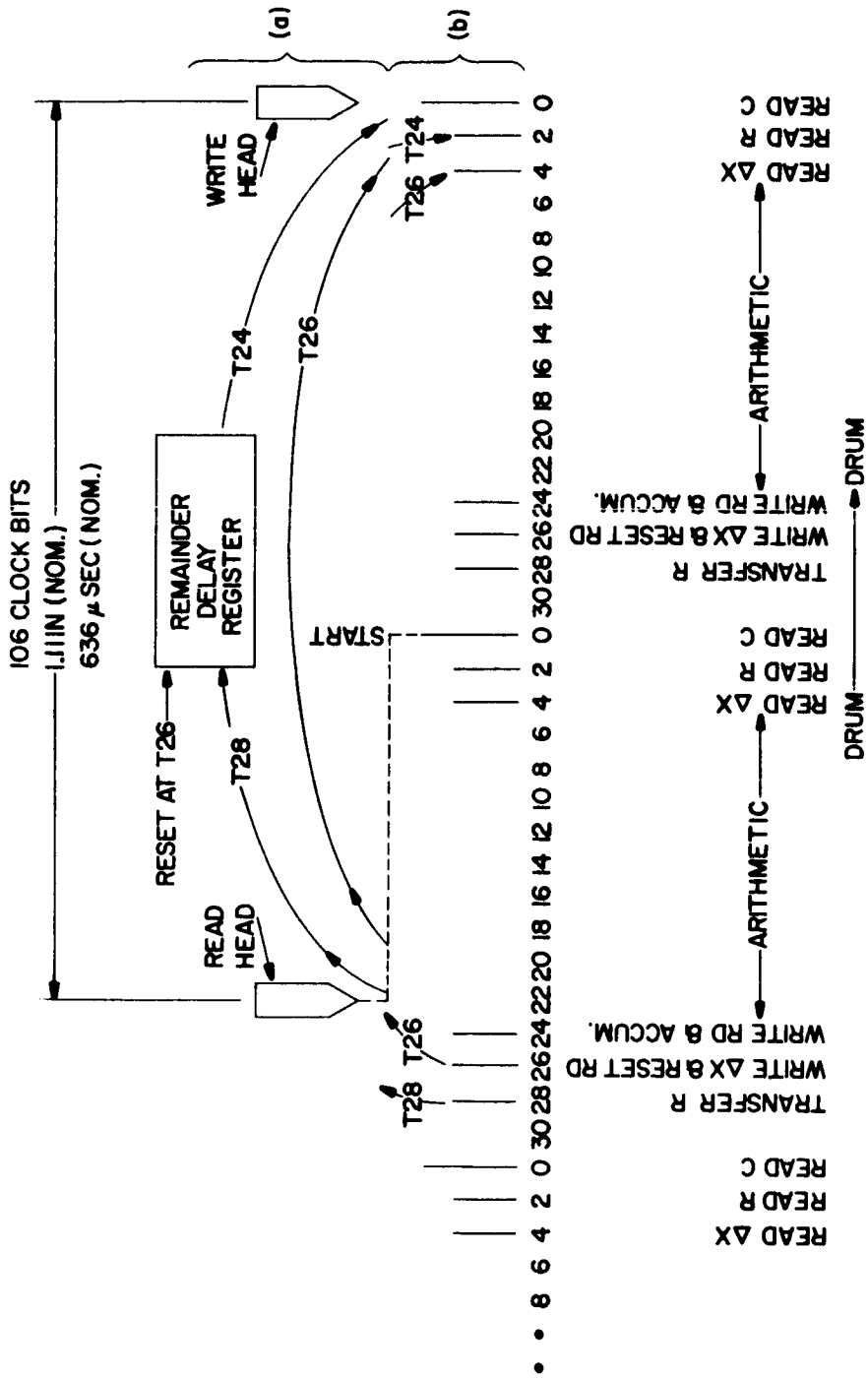


FIGURE 4-9 REMAINDER DELAY TIMING DIAGRAM

Table 4-2. During the time period of integrator 8, we need to form the actuating error and complete the processing of integrator 7. The timing is given in column 2 and will become self-explanatory later. During the time period of integrator 18, we complete the processing of integrator 17, change the contents of the sample and hold unit and reset the accumulator in preparation for the next cycle.

TABLE4-2-Clock Timing

Time	FUNCTION		
	Integrators 0 - 7 & 10 - 17	Integrator 8	Integrator 18
0	Read Const. (Prog. 1)	Read Input Command & Set Encoder	
1	Read Const. (Prog. 2)		
2	Read R		
3			
4	Read ΔX	Set Sign of ΔX to Sub.	
5			
6		Read Encoder	
7		Subtract	
8	Add		
9	Shift C & ΔX		
10	Add		
11	Shift C & ΔX		
12	Add		
13	Shift C & ΔX		
14	Add		
15	Shift C & ΔX		
16	Add		
17	Shift C & ΔX		
18	Add		
19	Shift C & ΔX		
20	Add		
21	Shift C & ΔX		
22	Add		
23	Shift C & ΔX		
24	Write R/D & Accum.	Write R/D & Set Error	Write R/D & Reset S&H
25			
26	Write X&Reset R/D	Write Error & Reset R/D	Write Accum, Trans To S&H & Reset R/D
27			
28	Transfer R		
29			
30	Reset	Reset	Reset Accumulator
31			

-ENABLE-

V DETAILED DESIGN OF THE DIGITAL COMPENSATOR AND PLANT SIMULATOR

In this chapter, we discuss the specifics of the present design. The timing, number system selected, the arithmetic unit, saturation error detector, registers and clock are discussed.

The cyclic and repetitious nature of the required caculations has been presented. It has been shown that a complete cycle requires the time of 18 integrators for the chosen amount of white noise rejection. The access time of the drum system determines the sample period. It is convenient to drive the drum at line frequency (3600 rpm) which gives a nominal sample period of 17 millisec. However, due to motor slip the sample period is 18 millisec.

The basic 12μ sec clock period is pressing the design value of 100 KC operation of both the drum and logic circuitry. However, the objective is for the digital compensator itself to possess a high frequency response so its compensation can result in high frequency plant performance, and still to exceed even this requirement by such a wide margin that the compensator can be time shared among many high frequency plants.

The constant register can accomodate an 18 bit word. The feedback encoders of the present plant have a range of 2^{16} or a resolution of 1 part in 65, 536. The actuating error subtraction operation must be completed in something less than the 12μ sec available. Also, each partial sum of the multiplication operation must be complete in the same time.

At the maximum velocity of the servomotor (3500 rpm) the maximum change in the actuating error, before it is sampled again 18 millisec later is 146 numbers which is less than 2^8 (256). The number system to be described later requires one additional place for sign so that for maximum capability the ΔX registers should accomodate 2^9 bit words. Since the product of two 9 bit numbers requires an 18 bit register for storage, the general storage requirements are compatible.

Addition and Subtraction

The binary number system chosen for the compensator is the two's complement.[10] A positive number is defined as an ordinary binary number where the excess register length to the left of the most significant bit contains ZEROES. If we subtract a positive number from zero, the result is called the two's complement of the number and may be used to represent the negative form of the number. As an example:

	SIGN BIT									
X_1 =	0	0	0	0	0	0	0	0	=	0
Y_1 =	0	0	0	1	0	1	1	0	=	+22
$X_1 - Y_1$ =	1	1	1	0	1	0	1	0	=	-22

Notice that a negative number is recognized by a ONE in the sign bit and a series of ONES in the bits of greater significance than the sign bit (if present).

The two's complement of a number Y may be found as follows

$$\text{two's complement } Y = 2^{n+1} - Y \qquad (5\text{-}1)$$

where n is the number of significant digits in the numbers being employed.

The particular property of the two's complement notation which we desire to use, is that we can perform addition without regard to the sign of augend or addend, and be sure the sum will be correct both in magnitude and sign. It can easily be proved that addition always gives us the correct result for any pair of numbers X and Y as follows. If the symbols X and Y each represent positive numbers, and we want to perform the addition X + (-Y), the sum will be represented by:

$$X + (\text{two's complement of } Y) = X + 2^{n+1} - Y = 2^{n+1} + (X - Y) \qquad (5\text{-}2)$$

We must now consider two possibilities:

1) If $X \geq Y$, then $X - Y \geq 0$ and the sum will be a positive number with 2^{n+1} added to it. Since 2^{n+1} is a ONE followed by

(n+1) ZEROES, it will have no effect on the sum or on the sign digit, and the sum will be correct.

2) If X<Y, then the sum will be $2^{n+1}-(Y-X)$, which is the two's complement of the positive number (Y-X).

We must still consider the addition of (-X) to (-Y). The representation of this sum will be

$$(-X) + (-Y) = 2^{n+1} - X + 2^{n+1} - Y = 2 \cdot 2^{n+1} - (X+Y) \qquad (5-3)$$

The 2 here appears to the left of the sign digit and will not actually appear in the result. The sum, therefore, will actually be indistinguishable from $2^{n+1}-(X+Y)$, which is the representation for the correct sum: $-(X+Y)$.

Our feedback encoder output is a positive natural binary number. The input command generator of the control unit, to be described later, is also a positive natural binary number. Therefore, this is one reason why our arithmetic unit must be capable of subtraction. Other reasons associated with the sign of ΔX and C will be presented later.

Multiplication can be performed by progressive shifting and adding. For example, consider

```
    1 1 0 1     Multiplicand      13
  × 0 1 0 1     Multiplier        ×5
  -------                         ---
    1 1 0 1                       65
    0 0 0 0     Partial Products
  1 1 0 1
0 0 0 0
-------
1 0 0 0 0 0 1   Product
```

Here, the multiplicand can be written into a shift register. For the first digit in the multiplier, ONE, the contents of the shift register can be read out to the accumulator (but not erased in the shift register). The contents of the shift register can then be shifted two places to the left (for the next multiplier, ONE) and again be read

out to the accumulator. At this point, the accumulator would have accumulated the entire product (sum of the shifted partial products) as

1 1 0 1	First entry and sum
+ 1 1 0 1 0 0	Second entry
1 0 0 0 0 0 1	Second and final sum

Division can be performed through complementing, shifting and accumulating. Thus with the proper sequence control, adders, subtractors, shift registers and accumulating registers can form the heart of an arithmetic unit. Hurley[11] gives one scheme of a logical adder accumulator which is reproduced in Fig. 5-1. The repeating sequence, when accumulating the sum of a column of numbers, is as follows:

1. Clear (P_1) addend register
2. Register (P_2) new addend bits
3. Allow time (say an empty pulse period P_3) for adders to add the accumulator and addend bits for all carries to propagate through all orders and be added properly i. e. allow time for the interconnected d-c level adder circuits of all orders to interact and their transients subside.
4. Clear (P_4) intermediate register
5. Transfer (P_5) sum bits to intermediate register
6. Clear (P_6) accumulator register
7. Transfer (P_7) sum bits from intermediate to accumulator register.

The intermediate register is required since the accumulator FF and the addend FF both supply inputs to the full adder. Without the intermediate register the new sum could change the accumulator state which in turn supplies a new input to the adder, and so on such that a form of instability could result.

Note that seven steps are required in this scheme. Where, in the present case, step 3 must be of a sufficient time duration to

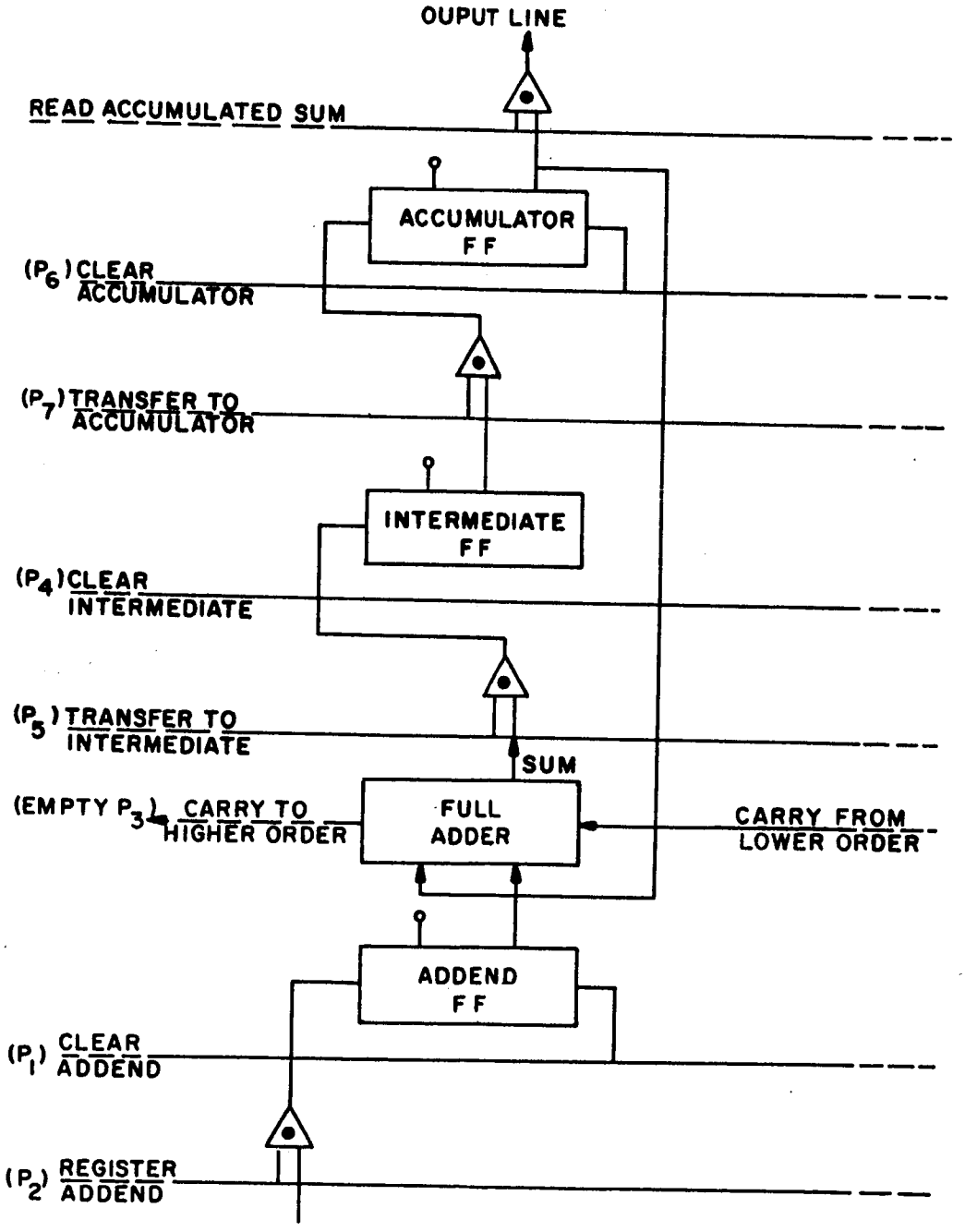


FIGURE 5-1 SCHEME OF A LOGICAL-ADDER ACCUMULATOR (FROM FIGURE 9-14 OF HURLEY [10])

allow the carries to ripple through 18 stages. These seven control steps must be accomplished in 12μsec if this scheme is used here.

Let us review the basic addition and subtraction truth tables to see if the intermediate register can be eliminated.

The truth table for the addition process is shown in Fig. (5-2) (a), where; K_i, is the addend, (K_i is the constant of the integrator); R_i is the augend, (R_i is the remainder quantity of the integrator,) C_i is the carry into a stage and C_{i+1} is the carry out of a stage.

We desire to place the new sum S, in the remainder register R_i. In order to try to eliminate the intermediate register, we ask, "Should the individual R_i flip-flop (FF) be changed so that it will contain the new sum, S?" Change R is represented by ΔR and the truth table column for it is shown in Fig. (5-2) (b).

Since we require a subtraction process, let us review this operation also. The truth table for subtraction is shown in Fig. (5-2) (c), where K_i is the subtrahend, R_i is the minuend, D_i is the difference, B_i is the borrow into a stage and B_{i+1} is the borrow out of a stage.

Again, we desire to place the new difference, D, in the remainder register R_i. We ask whether or not the individual R_iFF should be changed so that it will contain the new difference D. The truth table column of ΔR for the subtraction process is shown in Fig (5-2)(d).

Note that ΔR for both the addition and subtraction process is the same. Consequently, only one logic circuit is required for both operations.

It can also be seen that the addition carry, C_{i+1}, and the subtraction borrow, B_{i+1}, columns are different. A new quantity is formed which is

$$X_{i+1} = AC_{i+1} + \overline{A}B_{i+1} \qquad (5\text{-}4)$$

where A = add

and $\overline{A}$ = subtract

K_i	R_i	C_i	S	C_{i+1}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(a)

ΔR
0
1
0
1
1
0
1
0

X_{i+1}
0
0
0
1
0
1
1
1

(b)

K_i	R_i	B_i	D_i	B_{i+1}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	1

(c)

ΔR
0
1
0
1
1
0
1
0

(d)

0
1
0
0
1
1
0
1

(e)

FIGURE 5-2 TRUTH TABLES FOR ADDITION & SUBTRACTION

The truth table column for X_{i+1} is given in Fig (5-2) (e).

By noting, the opposite reflection about the dash-dot lines, it can be seen that the same truth table holds for the complement of each term.

From the truth table

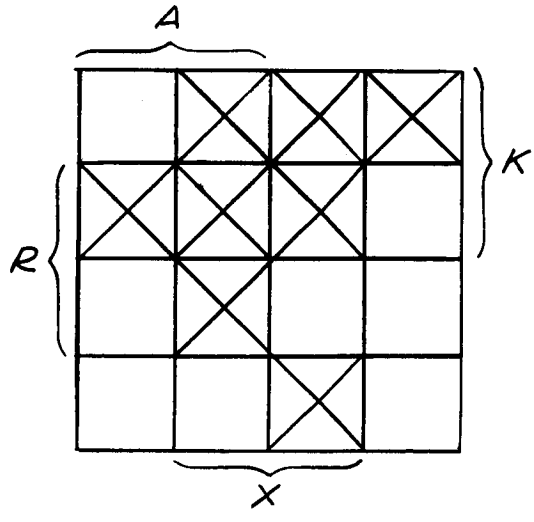
$$\Delta R_i = \overline{K}_i \overline{R}_i C_i + \overline{K}_i R_i C_i + K_i \overline{R}_i \overline{C}_i + K_i R_i \overline{C}_i$$

$$= (\overline{R}_i + R_i)(\overline{K}_i C_i + K_i \overline{C}_i)$$

$$\Delta R_i = (\overline{K}_i C_i + K_i \overline{C}_i) \qquad (5\text{-}5)$$

Thus, ΔR, can be constructed with an exclusive-OR circuit or an identity-not circuit.

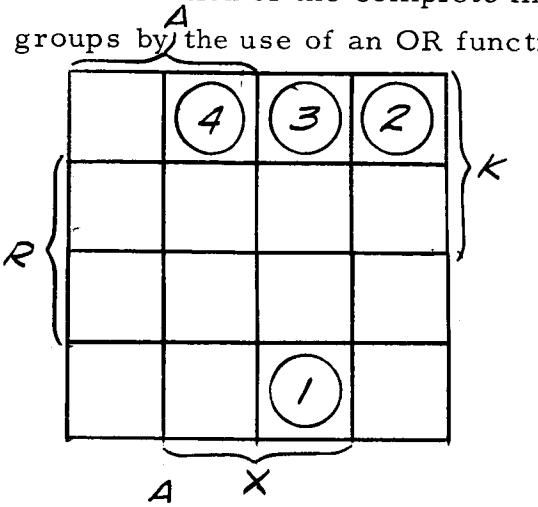
A Karnaugh map[11] for X_{i+1} is



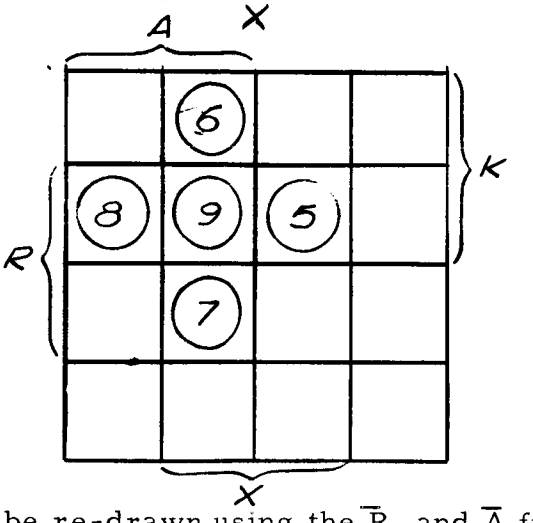
X_{i+1}

In order to minimize the carry propagation time for X_{i+1}, it is desirable to instrument, each carry circuit with passive resistors. However, each stage would be loaded down by its neighbor so this type of solution is not applicable to long register lengths. The best solution is a one transistor circuit wherein the transistor provides power gain and isolation.

The logical instrumentation of the complete map can be accomplished in two groups by the use of an OR function as shown below.

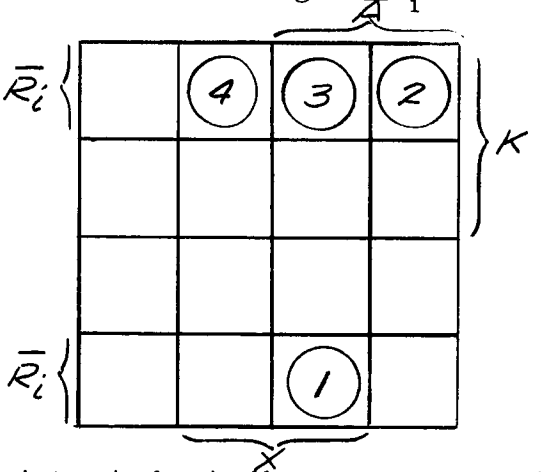


V_5



V_6

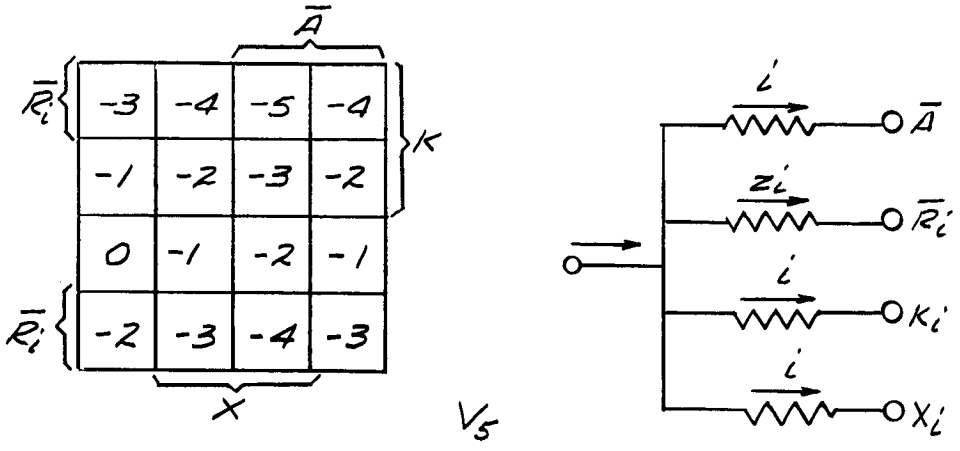
The map for V_5 can be re-drawn using the $\overline{R}_i$ and $\overline{A}$ function, i. e.



V_5

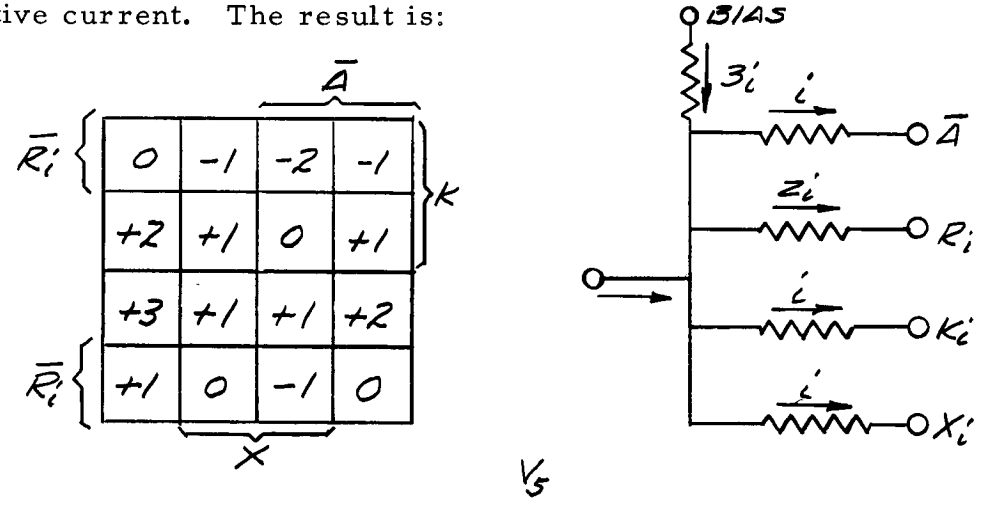
Since a transistor is basically a current amplifying device, we can modify the use of the Karnaugh map and use the modified map in conjunction with a passive resistor network. Since the

modified map has four variables our resistor network will have four inputs, i. e.



Where in each segment of the map we record the total current drawn for that particular set of inputs. An input draws current when TRUE and no current when $\overline{\text{TRUE}}$.

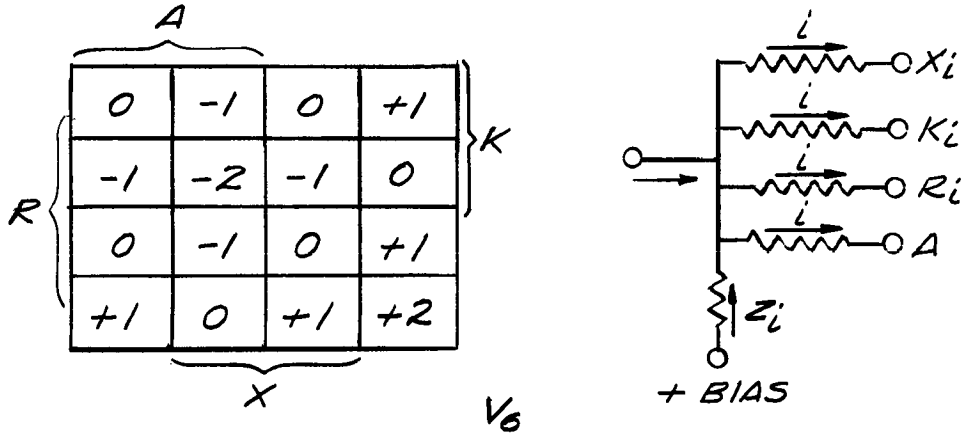
Next we add a source of bias current so the entire map can be raised or lowered. Here, let us bias the map with 3 units of positive current. The result is:



Now by using an npn-type transistor material, the transistor conducts when the current is minus and is cut-off when the current is near zero or positive. It can be seen that the segments with negative currents correspond to the original Karnaugh map for V_5.

This mapping technique has the advantage of establishing a ratio between the legs of our passive network. The inpedance level will depend upon the magnitude of the voltage sources available, the output impedance of the voltage sources, the transistor type, the i_c vs i_b curves of the particular transistor, etc. However, this simple technique quickly results in a trial circuit on which one can make a thorough analysis.

The map of V_6 and its passive network are given below:



Again notice only negative currents correspond to the desired map.

Since both maps have a range from +2i to -2i, the allowable tolerance on each leg is $\pm$ 12.5 per cent. The use of 5 per cent resistors allows for a variation in the Thevenin's equivalent of the current sources and a variation in transistor characteristics. With a closer control of tolerances maps of more variables and resistor legs can be constructed.

An OR function allows superposition of the maps to be applied. The OR function is implemented by means of diodes. The complete circuit and truth table is give in Fig 5-3.

The use of the diodes does increase the carry propagation time, but not very much. The nominal switching time of the transistor used (2N973) is 50 nanoseconds, while the conduction time of the diode (HD 1812) is 9 nanoseconds. The complete carry propagation time for an 18 digit register is nominally 1.1μ sec.

A	K_i	R_i	X_i	X_{i+1}
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1

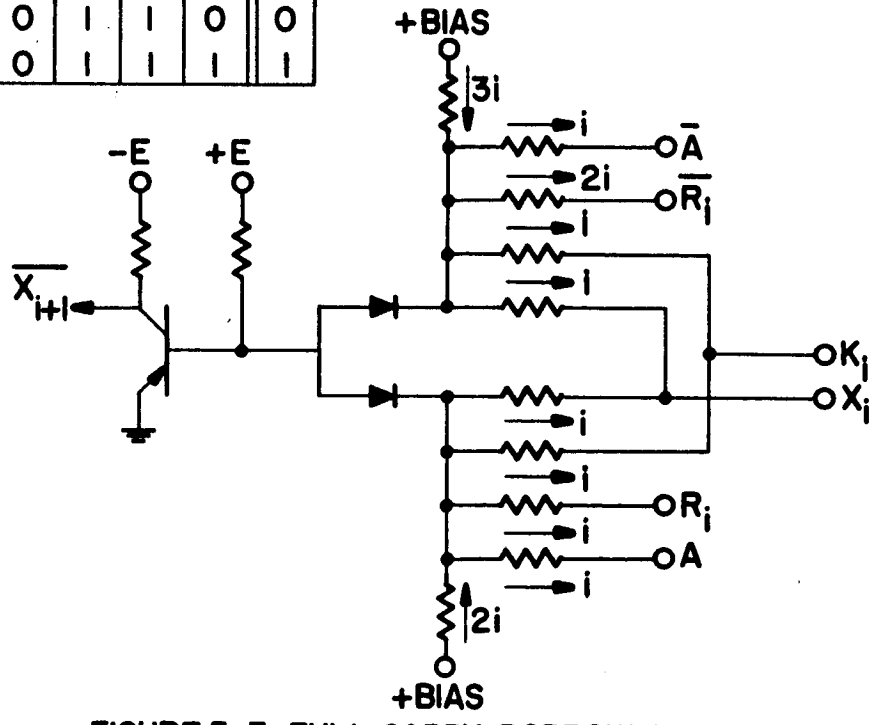
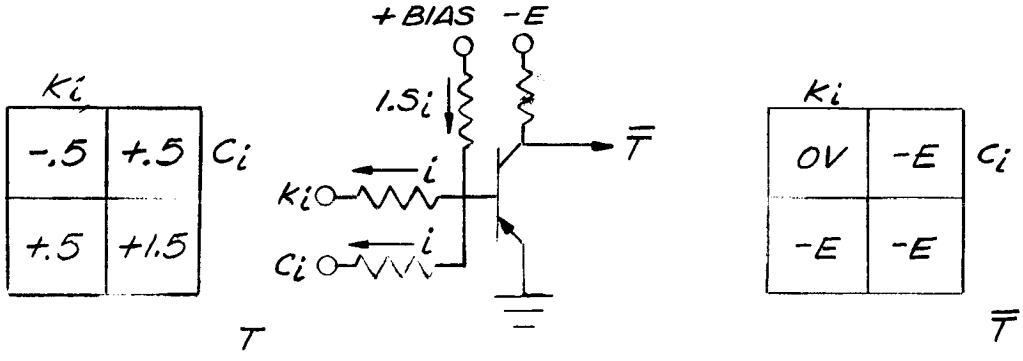


FIGURE 5-3 FULL CARRY-BORROW CIRCUIT

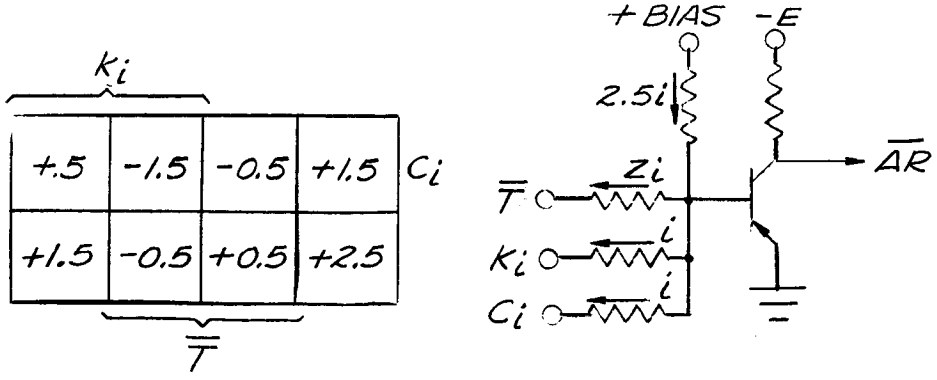
Note that $\overline{X}_{i+1}$ is obtained due to the inversion by the single transistor used. Alternate stages utilize the complement form of the inputs as allowed by the complementary symmetry of the truth tables. This is the reason that the register FF's alternate into the arithmetic unit in the detailed drawings shown later.

From eqn. (5-5) it can be seen that ΔR depends only upon the state of K_i and C_i. This is true, without regard for whether the arithmetic unit is adding or subtracing, or the state of R_i. It is the independence from the present state of R_i which makes possible the elimination of the intermediate register. As stated previously the ΔR circuitry can take the form of an exclusive-OR or an identity-not circuit.

A two variable map with bias and its passive circuit is as follows:



A three input map with bias and its passive circuit is as follows:



The ΔR transistor conducts under three conditions:

$$\text{Conduction} = K_i C_i \overline{T} + \overline{K}_i C_i \overline{T} + K_i \overline{C}_i \overline{T} = \overline{\Delta R} \qquad (5\text{-}6)$$

but $\overline{T} = \overline{K_i} + \overline{C_i}$

$$\therefore \text{ Conduction} = \overline{K_i} C_i + K_i \overline{C_i} = \overline{\Delta R} \qquad (5\text{-}7)$$

which is the desired exclusive-OR form. The complete circuit and truth table is given in Fig 5-4.

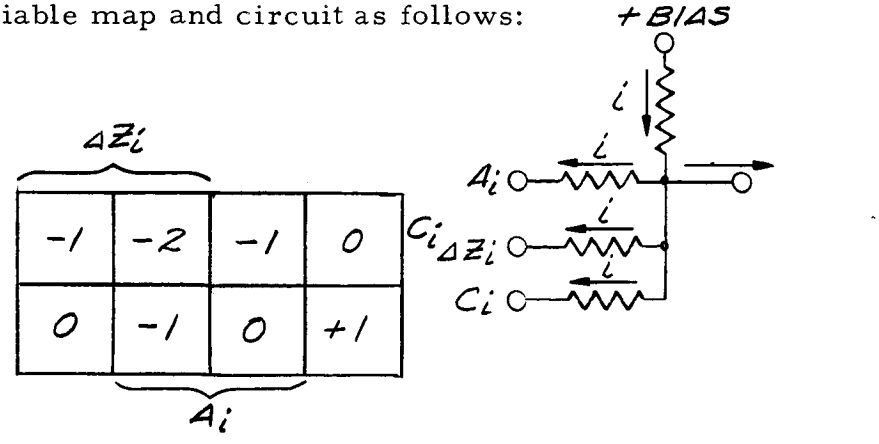
Notice that the truth table is complementary symmetric about the dash-dot lines. This means that the next stage in the register is the same as that shown except the complement of the inputs is used. This is in keeping with the fact that the register outputs alternate into the X_{i+1} circuits.

Accumulator Arithmetic Circuitry

Before discussing multiplication and completing the presentation of the integrator arithmetic unit, we can discuss the arithmetic circuitry used for the accumulator.

Since the numbers appearing in the ΔZ register are in two's complement form the only operation required of the accumulator arithmetic unit is addition. The truth table and circuitry for, change the accumulator, ΔA, is the same as that previously discussed for the ΔR. The carry circuit does not have to handle subtraction, so it can be simpler than that described for X_{i+1}.

The truth table for C_{i+1} is given in Fig (5-2) (a) and (b). The names of the variables are changed however, where ΔZ_i replaces K_i and A_i replaces R_i. This truth table requires a three variable map and circuit as follows:



A	K_i	R_i	X_i	ΔR
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0

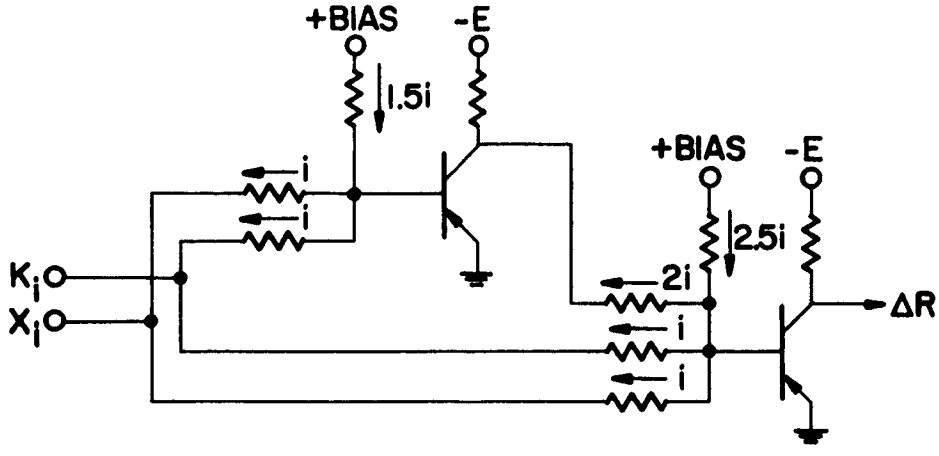


FIGURE 5-4 FULL SUM-DIFFERENCE CIRCUIT

Notice, that the negative currents correspond to the truth table and that there is complementary symmetry again about the dash-dot line. The truth table and circuit for the complete adder is given in Fig 5-5. The accumulator logic diagram is given in Fig 5-6.

Multiplication

Multiplication based upon shifting and addition has been described previously. The register used to contain the multiplicand, our constant coefficient in the integrator case, is shown in Fig 5-7. This register must be capable of shifting the constant coefficient to the left. Accordingly, the constant register is a unidirectional shift register with steered carries. When a shift command pulse occurs, the information in the shift register is to be simultaneously transferred to the next flip-flop in the register. That is, the value of the i^{th} digit before the shift pulse, (P_{SH}) is to be that of the $(i+1)$ digit after the shift pulse. Using an RS flip-flop, the logical equations used are

$$R_{i+1} = R_i(P_{SH}) = \overline{S}_i\,(P_{SH})$$

$$S_{i+1} = S_i(P_{SH}) = \overline{R}_i\,(P_{SH}) \qquad (5\text{-}8)$$

The flip-flops are connected through steering gates to the next flip-flop as shown. The outputs of the flip-flops are connected to the level input of the steering gate. The diode of the steering gate is connected to the base of the transistor on the opposite side of the next flip-flop. The shift pulse is applied to the capacitor inputs of all steering gates simultaneously.

The ΔX register, (Fig 5-8) is an identical design except the information shifts to the right.

In order to process an integrator arithmetically we need to carry out the logical equation given as eqn. (4-2) and repeated here for convenience.

$$\Delta Z[nT] + R[nT] = y[nT]\,\Delta X[nT] + R[(n-1)T] \qquad (4\text{-}2)$$

ΔZ_i	A_i	C_i	ΔA	C_{i+1}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

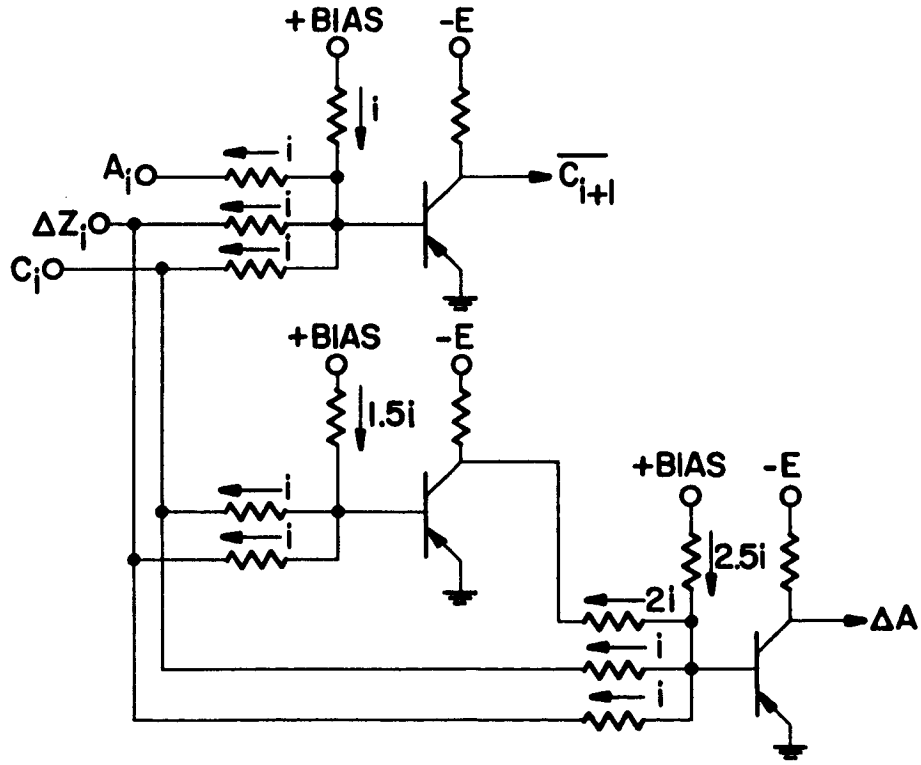


FIGURE 5-5 FULL ADDER CIRCUIT

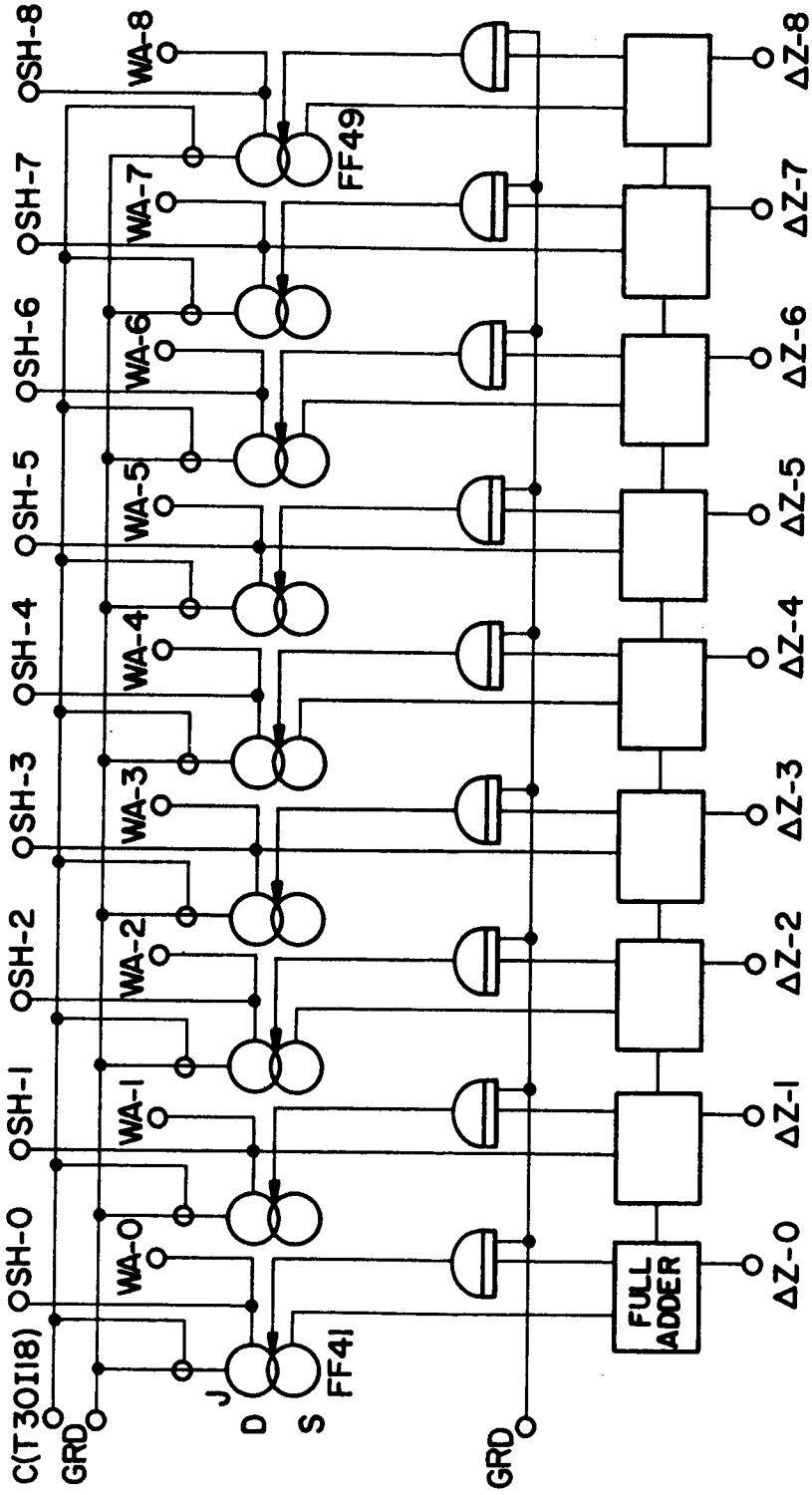


FIGURE 5-6 ACCUMULATOR LOGIC DIAGRAM

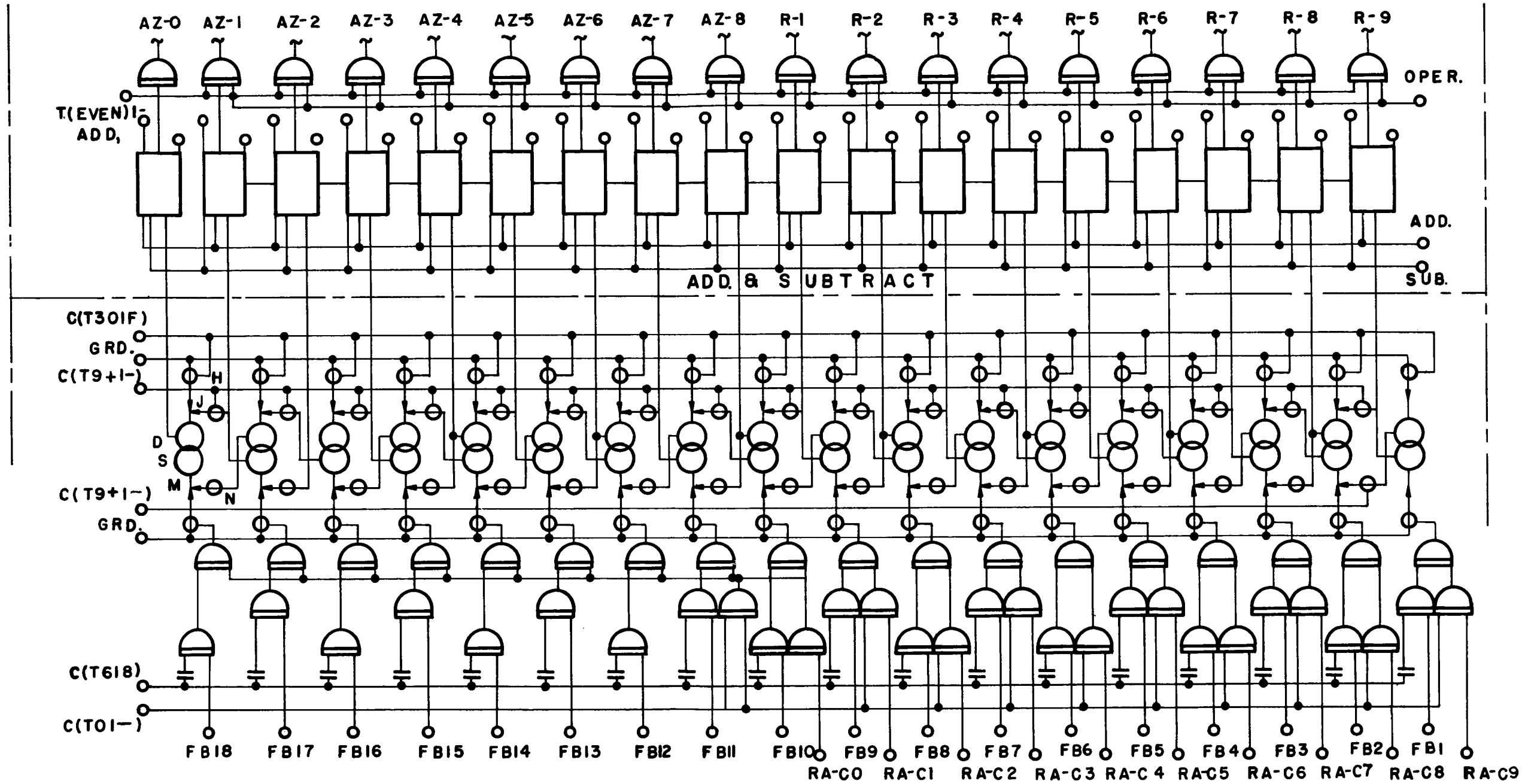


FIGURE 5-7 CONSTANT REGISTER AND ADDER-SUBTRACTOR LOGIC DIAGRAM

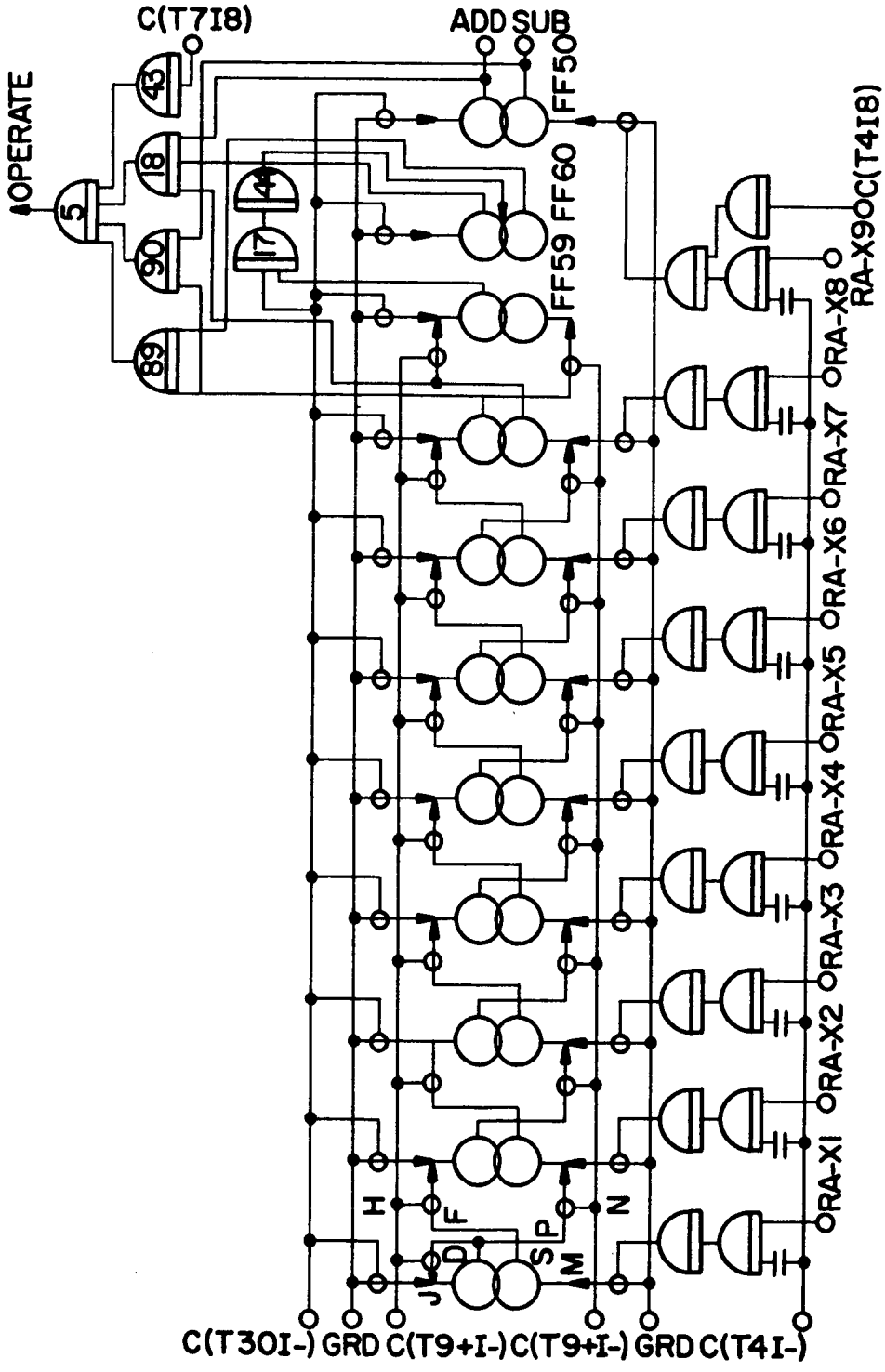


FIGURE 5-8 ΔX REGISTER LOGIC DIAGRAM

The right side consists of a multiplication and the addition of the product to the past remainder. The past remainder is read into the R register prior to starting the multiplication. The partial products are then added to this past remainder later to accomplish the right side of eqn (4-2).

At the proper clock time the constant, $Y(nT)$ and $\Delta X(nT)$ are read from the drum into their respective registers. What we need is an algorithm to control the multiplication.

There are four possible cases: $+C$ and $+\Delta X$; $+C$ and ΔX; $-C$ and $+\Delta X$; and $-C$ and $-\Delta X$. Both the C and ΔX values are in twos complement form. Let us assume that ΔX is in sign and magnitude form and that the sign of ΔX determines the operation of addition or subtraction. Let the value of C be 3 and the value of X be 5 and study the four cases.

$$
\begin{array}{rcccccccc}
C = +3 & = & & & 0 & 0 & 0 & 1 & 1 \\
\Delta X = +5 & = & & & & 0 & 1 & 0 & 1 \\
\hline
+15 & & & & 0 & 0 & 0 & 1 & 1 \\
 & & 0 & 0 & 0 & 1 & 1 & & \\
\hline
 & & 0 & 0 & 0 & 1 & 1 & 1 & 1 \quad = +15
\end{array}
$$

Since the sign of ΔX is plus, the operation is add, so that a +15 is added to the previous remainder, which is correct.

$$
\begin{array}{rcccccccc}
C = +3 & = & & & 0 & 0 & 0 & 1 & 1 \\
\Delta X = -5 & = & & & & 0 & 1 & 0 & 1 \\
\hline
-15 & & & & 0 & 0 & 0 & 1 & 1 \\
 & & 0 & 0 & 0 & 1 & 1 & & \\
\hline
 & & 0 & 0 & 0 & 1 & 1 & 1 & 1 \quad = +15
\end{array}
$$

Since the sign of ΔX is minus, the operation is subtract, so that a +15 is subtracted from the previous remainder, which is correct.

C = -3	=			1	1	1	0	1	
ΔX = +5	=				0	1	0	1	
-15				1	1	1	0	1	
		1	1	1	0	1			
	1	0	0	1	0	0	0	1	= -15

Sign the sign of ΔX is plus, the operation is add, so that a -15 is added to the previous remainder which is correct.

C = -3	=			1	1	1	0	1	
ΔX = -5	=				0	1	0	1	
				1	1	1	0	1	
		1	1	1	0	1			
	1	0	0	1	0	0	0	1	= -15

Since the sign of ΔX is minus, the operation is subtract, so that a -15 is subtracted from the previous remainder, which is correct.

What we desire then, is to let the sign of ΔX control the operation and change the two's complement magnitude to magnitude only form. One rule for changing from two's complement form to magnitude only is

> "Leave all initial ZEROES alone, subtract the first ONE from two, and change all subsequent digits."

Conversion of the number with this rule requires precious time. Let us state a new rule which would require no time. The rule

is

1) Let the operation be determined by the sign of ΔX, i.e.
   A) if plus, ADD
   B) if minus, SUBTRACT

2) A) If ΔX is plus, the operation should occur on each ONE.
   B) If ΔX is minus, the operation should occur on the first ONE, and on each ZERO thereafter of the magnitude of ΔX.

When ΔX is plus, the previous examples suffice. Let us use the new rule for multiplication when the ΔX are minus. Note that minus ΔX values are in two's complement form.

```
C = +3      =        0 0 0 1 1
X = -5      =          1 0 1 1     = -5
  -15              0 0 0 1 1
              0 0 0 1 1
            0 0 0 1 1 1 1         = +15
```

Since the sign of ΔX is minus, the operation is subtract, so that a +15 is subtracted from the previous remainder.

```
C = -3      =        1 1 1 0 1
X = -5      =          1 0 1 1
  +15              1 1 1 0 1
            1 1 1 0 1
          1 0 0 1 0 0 0 1         = -15
```

Since the sign of ΔX is minus the operation is subtract, so that a-15 is subtracted from the previous remainder, which is correct.

It remains to logically implement our new rules. To do this, we implement a quantity, (AFTER FIRST ONE). A ONE in the magnitude of ΔX is denoted by ΔX. A ZERO in the

magnitude of ΔX is denoted by $\overline{\Delta X}$. The plus sign of ΔX is denoted by (+) and the minus sign of ΔX by (-). The operation rule can be stated as follows:

$$\text{OPERATE} = X(+) + \overline{X}(-)\,[\overline{\text{AFTER FIRST ONE}}] + \overline{X}(-)\,[\text{AFTER FIRST ONE}] \qquad (5\text{-}9)$$

$$= X(+) + X[\overline{\text{AFTER FIRST ONE}}] + \overline{X}(-)[\text{AFTER FIRST ONE}]$$

The quantity (AFTER FIRST ONE) is instrumented as shown with the ΔX register in Fig 5-8. The sign of ΔX is placed into the FF on the extreme right where it controls the operation A or $\overline{A}$ of the arithmetic circuitry. ΔX requires eight digits plus sign so FFs 59 & 60 are used for the quantity (AFTER FIRST ONE). FF60 is TRUE after the first one is shifted from FF58 to FF59. The first term of eqn (4-9) is instrumented by NOR element 90. When the first ONE is shifted into FF59 and the (AFTER FIRST ONE) flip-flop has not previously been energized and a shift pulse is present, FF60 is triggered. The first termof eqn (4-9) is instrumented by NOR element 89 and the third term by element 18.

By referring to the arithmetic block diagram in Fig 5-7, the OPERATE signal is required to gate the ΔR signals into the R register. The arithmetic circuitry makes an addition or subtraction each clock period, but the result is not transferred to the remainder register unless the ΔX control

permits it.

Notice that by using these rules no time was used to convert from two's complement to magnitude only form. An operation occurs on the first ONE in either case and the ΔX quantity has to be shifted anyway. The quantity (AFTER FIRST ONE), is TRUE for the complete ΔX word and is reset before the next ΔX quantity arrives.

Thus, by the use of passive resistor arithmetic circuits and the new rules for multiplication, (which includes division), an arithmetic unit of minimal components and therefore, extreme speed was developed.

Multi-Increment Integrator

The multi-increment integrator consists basically of the constant, ΔX and ΔZ-remainder registers and the arithmetic unit. The basic block diagram was presented in Fig (4-4). To be economical of equipment the registers and arithmetic unit are time shared between all 18 integrators. This is accomplished by storing the constant, ΔX, and remainder values in the memory unit until it is time to process the integrator. In accordance with the clock timimg,, Table4-2,the read amplifier transfers the constant value from the drum into the constant register (see Fig (5-7). The ΔX value is then transferred from the drum into

ΔX register (see Fig 5-8). Then the previous remainder value is transferred from memory to the ΔZ-remainder register. The arithmetic unit multiplies C by Δx and adds the result to the ΔZ-remainder register. The processing of the multi-increment integrator is now complete except for utilizing the new ΔZ result and returning the new remainder to storage.

The new ΔZ result is accumulated in the accumulator register (see Fig 5-6) in accordance with the compensation diagram, Fig (4-6). The new remainder is temporarily delayed in the remainder delay register, Fig 5-9, in accordance with the remainder delay timing diagram, Fig 4-9.

The new ΔX and remainder values are returned to storage by the write amplifier logic shown in Fig 5-10. The registers are reset and the next integrator is then processed in a similar manner.

Non-Linear Saturation Error Logic

As discussed earlier, the overflow, ΔZ, from integrator , become the ΔX command of integrator (i-1). (See Fig 4-6). The number of multiple lines allowed for this purpose is eight for magnitude and one for sign. Also, as has been discussed, the original source of these ΔX commands is the servo error computed during the time period of integrator eight.

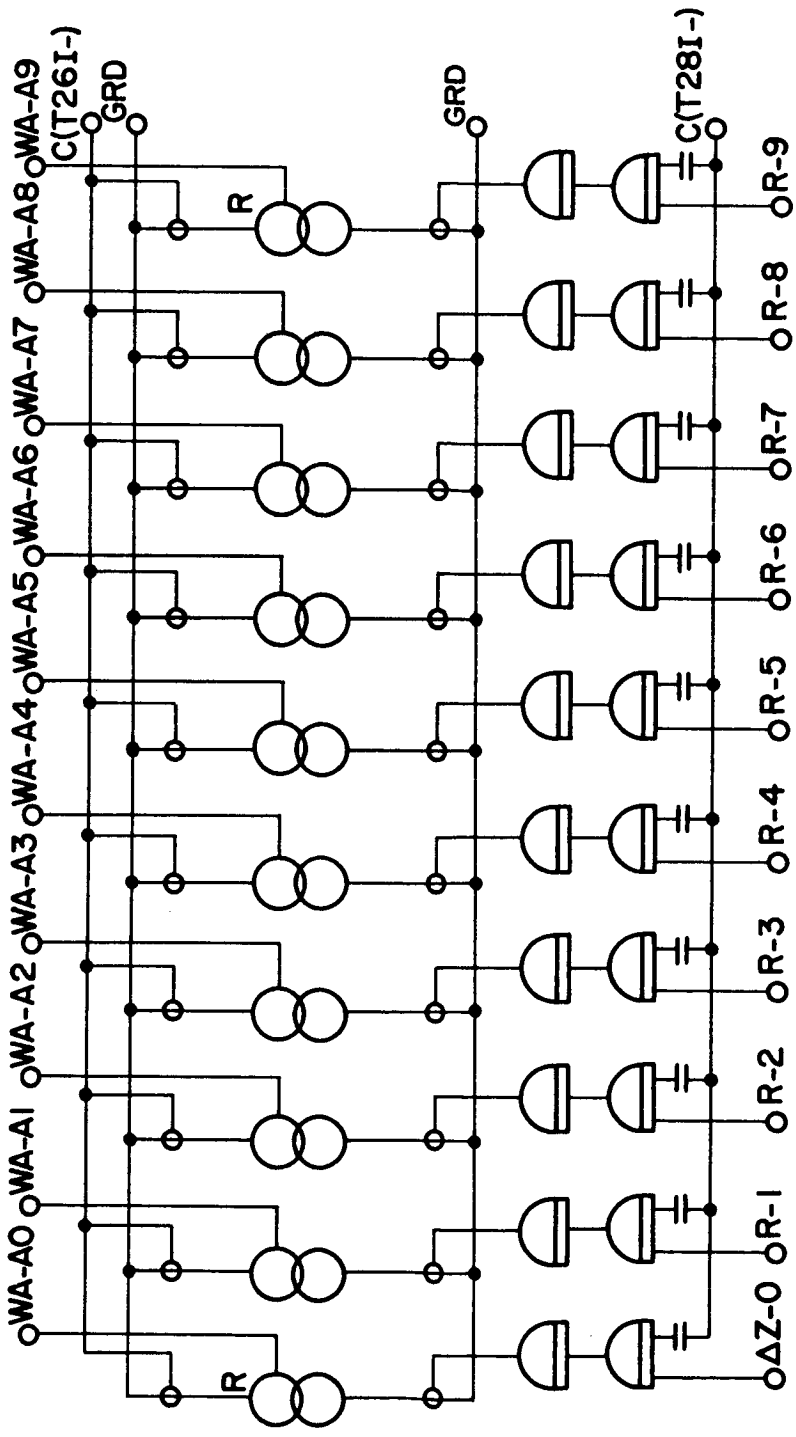


FIGURE 5-9 REMAINDER DELAY REGISTER LOGIC DIAGRAM

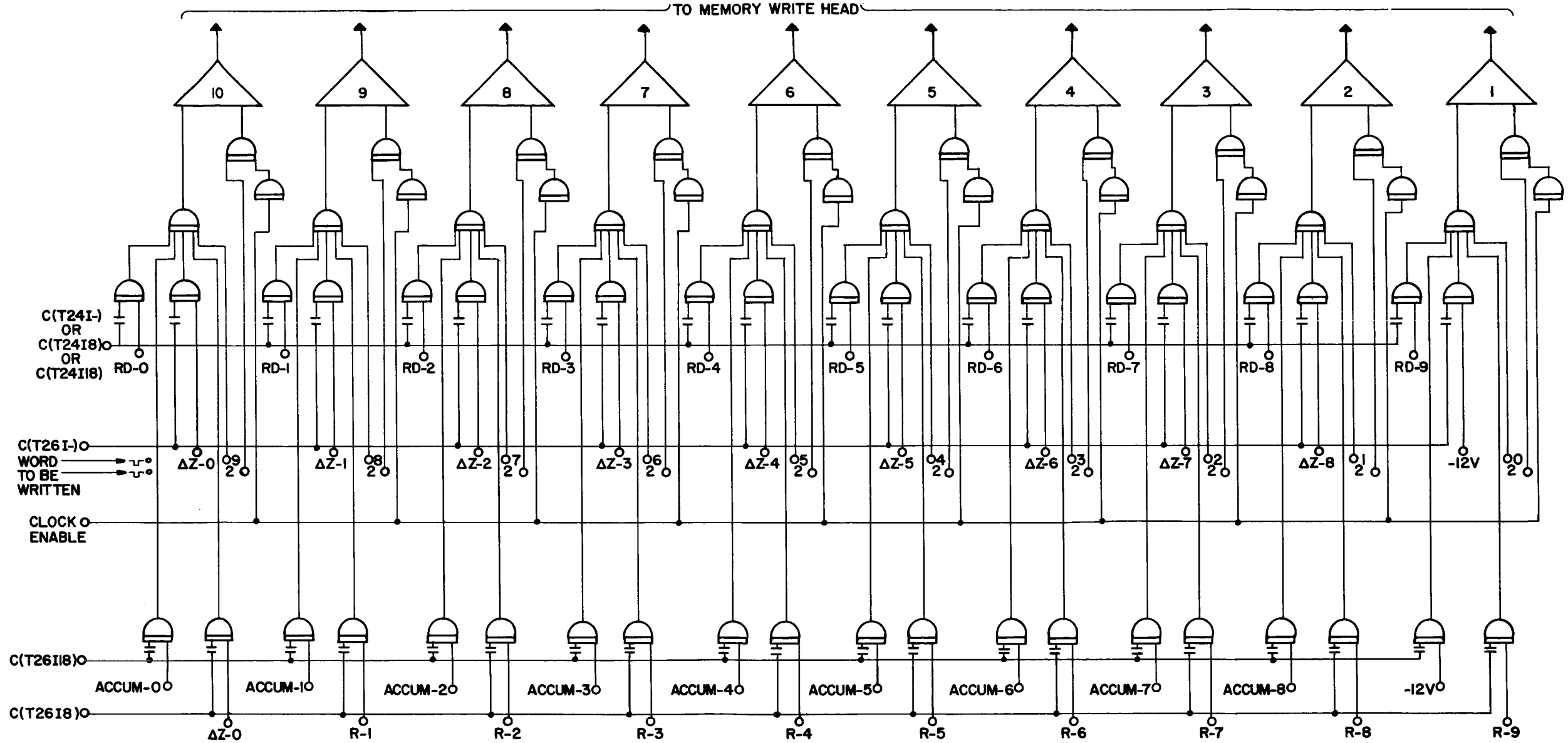


FIGURE 5-10 WRITE AMPLIFIER LOGIC DIAGRAM

At clock time zero of integrator eight, C(T0I8), the input command is read into the remainder register by means of the gates shown in Fig 5-11 and in accordance with the clock timing diagram given in Table 4-2. At C(T6I8) the feedback encoder is read into the constant register and during C(T7I8) the actuating error is computed and placed in the lower part of the remainder register.

Since the range of the feedback encoders is 2^{16}, it should frequently happen (as in the case of step-function inputs) that the actuating error would exceed 2^{9}. However ΔX is capable of receiving only 9 digits. If nothing were done, an actuating error of 2050 parts would be placed into integrator 7 as a ΔX command of only 2.

Maximum possible performance would be obtained from the plant if the servomotor is commanded to reduce the error at its maximum saturated speed. Accordingly, we desire that the ΔX be the maximum possible value of the correct sign whenever the actuating error exceeds the linear range of the compensator.

Register position 17 is the sign digit of the input command and feedback encoder registers. Recall from the discussion of the two's complement that a negative number is characterized by a train of one's after its most significant digit.

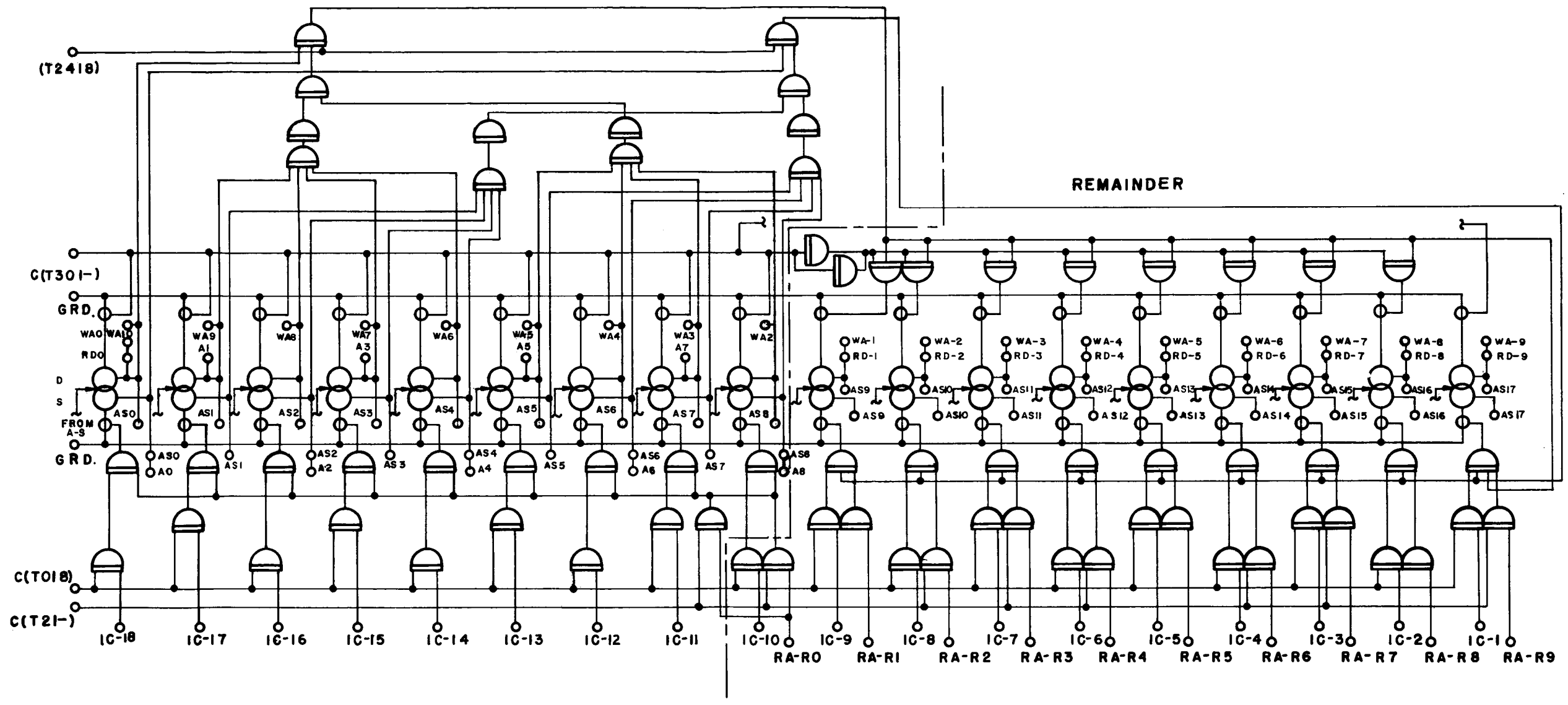


FIGURE 5-11 ΔZ— REMAINDER REGISTER AND SATURATION ERROR LOGIC DIAGRAM

There are four cases we need to instrument.

1) If FF17 is ZERO, and all FF's from 9 through 16 are ZERO, the actuating error is within the linear range and positive.

   In this case we write the contents of the remainder register for ΔX and write a plus sign.

2) If FF17 is ZERO, any of the FF's from 9 through 16 are ONE, the actuating error is big and positive.

   In this case we write all ONES for ΔX (our largest positive value) and write a plus sign.

3) If FF17 is a ONE, and all FF's from 9 through 16 are ONES, the actuating error is within the linear range and negative.

   In this case, we write the contents of the remainder register for ΔX and write a negative sign.

4) If FF17 is a ONE, and any of the FF's from 9 through 16 are ZERO, the actuating error is big and negative.

   In this case we write a ONE in the LSD and all ZEROES in the remaining digits (our largest negative value) and write a negative sign.

The logic is instrumented by means of AND gates where the outputs set or reset the remainder FF's as required in cases 2 and 4. Nothing is done in cases 1 and 3 since the result is a normal occurrence. These circuits are operative during C(T24I8), set error.

This non-linear saturation feature is very important in order to obtain the maximum dynamic performance from the plant.

Clock Design

The magnetic drum is the reference for the complete system. Each quantity taken from and returned to storage must be located precisely. Since changes in line voltage cause changes in drum speed, there is a train of pulses magnetized into one track of the drum which serve as the basic clock reference. As the drum rotates, the read amplifier associated with the clock track feeds a train of pulses into the counter shown in Fig (5-12). Combinational circuitry from this counter serves to build the clock pulses required in Table 4-2 and discussed previously.

The basic design problem is to obtain the required clock pulses without overloading the logic elements.

By dividing an integrator period into 32 parts the same counter is merely extended to count integrator positions. Since the integrator subinterval time periods are used repeatedly, they are merely AND gated with the integrator number.

One line accommodates integrators 0 through 7 and 10 through 17. This line is termed I- .

A Karnaugh map can be drawn for this line as follows:

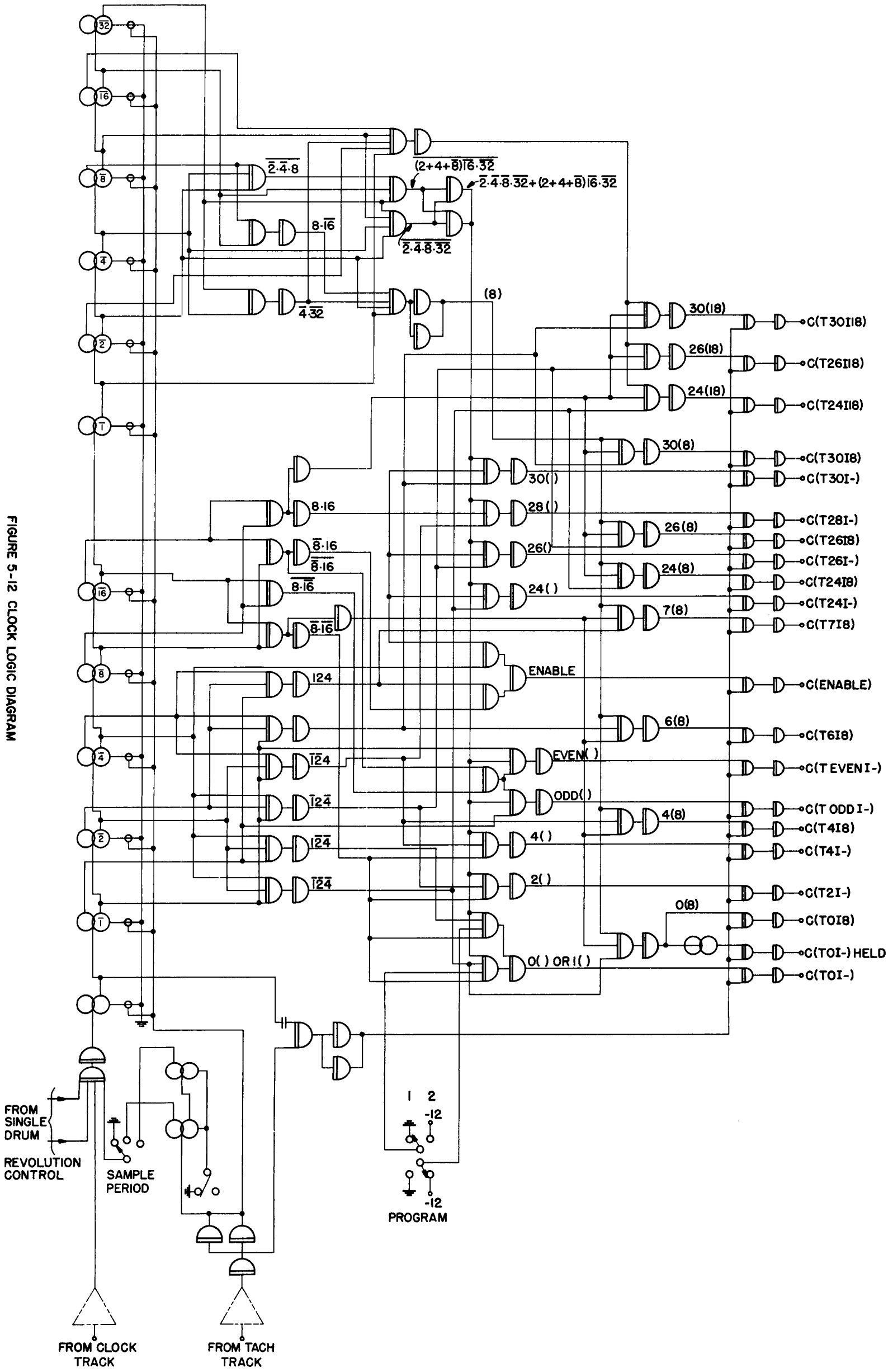
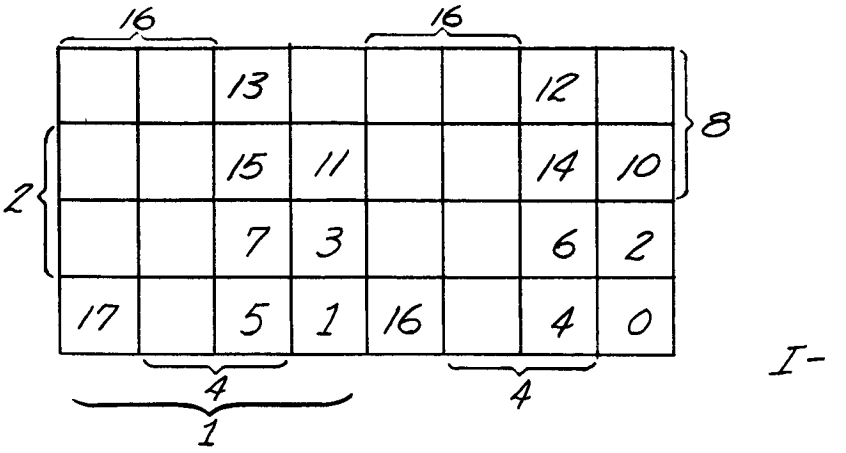


FIGURE 5-12 CLOCK LOGIC DIAGRAM



$$I^- = \overline{32}\ \ \overline{16(\bar{1}\ \bar{2}\ \bar{4}\ \bar{8})(\bar{1}\ \bar{2}\ \bar{4}\ \bar{8})} + \bar{4}\ \bar{8}\ \bar{2}$$

$$= \overline{32}\ \ \overline{16}(1+2+4+\bar{8})(\bar{1}+2+4+\bar{8}) + \bar{4}\ \bar{8}\ \bar{2}$$

$$= \overline{32}\ \ \overline{16}(2+4+\bar{8}) + \bar{4}\ \bar{8}\ \bar{2}$$

$$I^- = \bar{2}\ \bar{4}\ \bar{8}\ \overline{32} + (2+4+\bar{8})\overline{16}\ \overline{32} \qquad (5\text{-}10)$$

The various combinational elements for the function are shown in Fig 5-12.

The others are done in a similar manner with their combinational elements also marked in the same figure.

Since each of the quantities does not pass through the same number of logic gates they are available at slightly different times at the output. A series of AND gates are used at the output to again reference these clock pulses with the drum before they are emitted.

A second track on the drum surface which con-

tains only a single pulse serves as a "tach" pulse. This "tach" pulse resets the counter to zero each time it passes.

Other features of the clock design will be described later.

Design of the Digital to A-C Converter

The digital plant to be described is driven by a high performance instrument two phase A-C servomotor. The digital compensator described previously is applicable to most any plant. The one built here is an attempt to simulate a plant of high dynamic performance capabilities. The use of an A-C carrier system does raise some interesting points which are discussed below.

Although the compensation theory presented is designed to reduce the system time constants including those of the power element, the techniques are not enough to provide adequate torque and/or speed if these factors are not inherently present in the basic system design.

The choice of whether the form of the power element is to be electric, hydraulic, pneumatic, or some other is frequently based on factors other than performance considerations alone. Weight, size, cost and reliability are other factors that may

dictate the form of the power element. The primary reasons for using A-C servomechanisms is econony of components, cost and weight.[12]

D-C motors are powered by D-C servoamplifiers which are subject to drift as well as being sensitive to other factors. These are disadvantageous to A-C systems also. To convert D-C to an A-C signal, modulators are sometimes used, the modulator output may not be a pure sinewave. The frequency range of the information that can be transmitted tends to be more limited and there is a limited amount of change in the frequency of the reference (carrier) signal that can be tolerated without a deterioration of the control performance. Changes in the carrier frequency do not affect the numerical compensation nor the digital to A-C converter developed.

The function of the digital to A-C converter is to take the number in the sample and hold register, Fig 4-8 & 5-13, and convert it to an amplitude modulated phase sensitive A-C carrier signal. In this case the carrier is 60 cps. The circuit developed is shown in Fig (5-14).

The state of each FF serves to either open or close a gate formed by the two diodes. The gate is open when current flows from the FF through the diodes. The 60 cps carrier is added to the signal flowing through the gate by means of the capacitor.

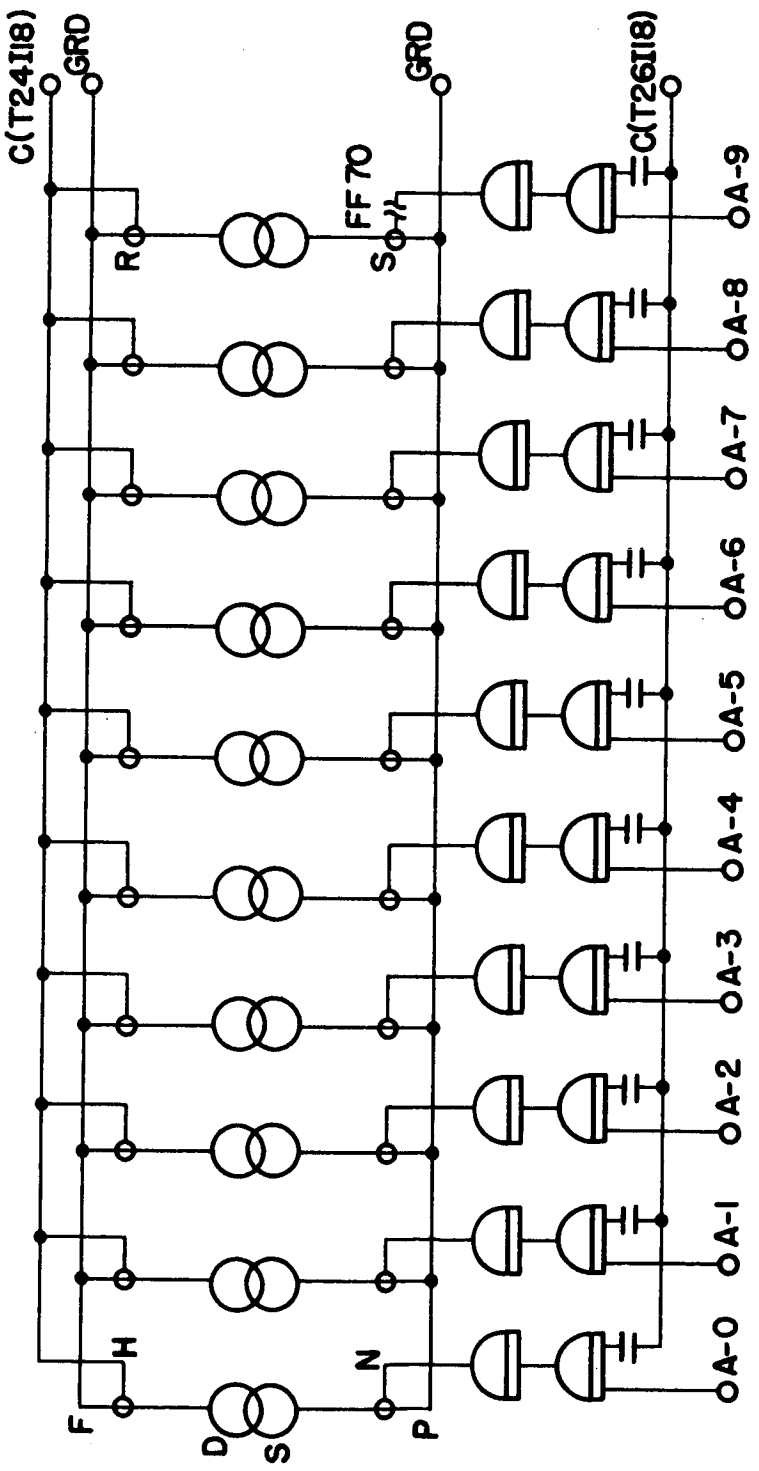


FIGURE 5-13 SAMPLE AND HOLD REGISTER LOGIC DIAGRAM

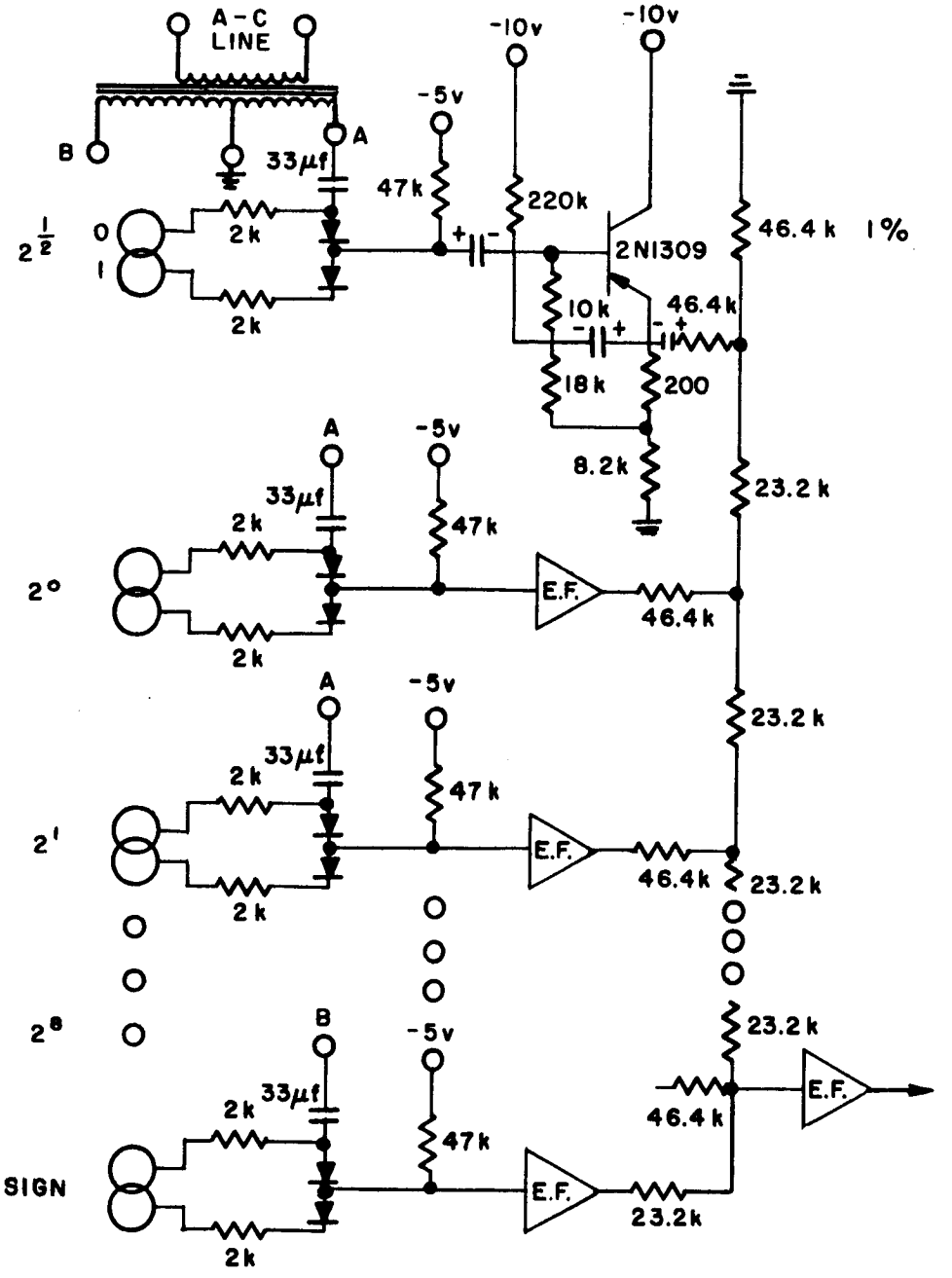


FIGURE 5-14 DIGITAL TO A/C CONVERTOR

The design requirement is that the current from the FF exceed that from the capacitor. Under this condition there is always a net current through the diodes and they remain open. When the FF is in the reverse state, it back biases both doides in series and the attenuated signal from the capacitor tends toward zero. The purpose of the -5V bias is to maintain the potential of the junction between the diodes to this value. Without the bias, the junction potential is uncontrolled and any transient changes would pass through the emitter follower stages. The emitter follower stages[13] present a high impedance load to the diode gates and a low impedance voltage output to the normal voltage source ladder network.[14] The novel feature here is the means of handling the phase of the carrier with the sign of the number stored and obtaining the output voltage with respect to ground.

A 60 cps voltage of equal magnitude but of the opposite phase is taken from the other half of the center-tapped transformer (terminal B). This opposite phase signal is gated through the sign FF in the same manner as the other gates. Thus when the value stored in the sample and hold register is negative, the gate associated with the sign bit conducts and applies a voltage of equal magnitude but opposite phase to the additional resistor added to the voltage ladder.

The Thevenin's equivalent of the voltage ladder alone is

$E(\phi_{in})$ x (Sum) —R/2→

where $E(\phi_{in})$ = magnitude of in-phase carrier voltage

and

$$\text{Sum} = d_0 2^0 + d_1 2^1 + d_2 2^2 + \ldots\ldots + d_n 2^n$$

d_i = ZERO or ONE

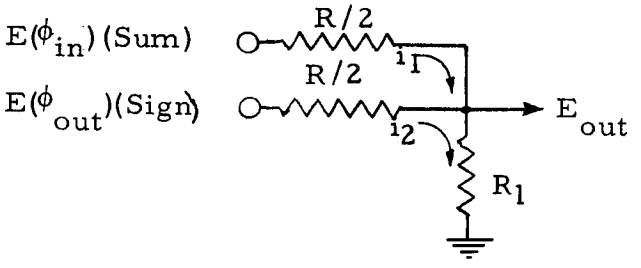
The Thevenin's equivalent of the sign bit circuit above is

$E(\phi_{out})$ x (Sign) —R/2→

Where $E(\phi_{out})$ = magnitude of out-of-phase carrier voltage

and Sign = ZERO or ONE if the magnitude is positive or negative, respectively.

The voltage into a finite load becomes:



$$E_o = R_2 (i_1 + i_2) \qquad (5\text{-}11)$$

$$\text{where } i_1 = \frac{E(\phi_{in})(\text{Sum})}{\frac{R}{2} + \frac{RR_1}{R+2R_1}} \quad \text{and} \quad i_2 = \frac{E(\phi_{out})(\text{Sign})}{\frac{R}{2} + \frac{RR_1}{R+2R_1}}$$

$$\therefore E_o = K\left[E(\phi_{in})(\text{Sum}) + E(\phi_{out})(\text{Sign})\right] \qquad (5\text{-}12)$$

where

$$K = \frac{R_1}{\frac{R}{2} + \frac{RR_1}{R+2R_1}}$$

$$\text{but } |E(\phi_{in})| = |E(\phi_{out})|$$

$$\therefore E(\phi_{out}) = -E(\phi_{in}) \qquad (5\text{-}13)$$

also, since the sign bit is located in the (n+1) FF it has a value equivalent to 2^{n+1}. If we let the Sum = Y, eqn (5-12) can be written..

$$E_o = KE \left[Y - 2^{n+1} (Sign) \right]$$

or

$$E_o = -KE \left[2^{n+1} (Sign) - Y \right] \qquad (5\text{-}14)$$

This is in keeping with our definition of the two's complement (see eqn (5-1)). When the Sign is ZERO

$$E_o = KE \left[Y \right] \qquad (5\text{-}15)$$

and the output voltage is an inphase carrier magnitude proportional to the sum Y. When the Sign is ONE

$$E_o = - KE \left[2^{n+1} - Y \right] \qquad (5\text{-}16)$$

$$= - KE \left[\text{two's complement Y} \right]$$

and the output voltage is an out-of-phase carrier magnitude proportional to the two's complement of Y which is the value in the register when the sign is a ONE.

Design of the Servoamplifier

The function of the servoamplifier is to amplify the amplitude modulated 60 cps carrier, to provide a variable system gain, and to convert the signal to a power form for application to the motor.

The servoamplifier schematic is shown in Fig 5-15.

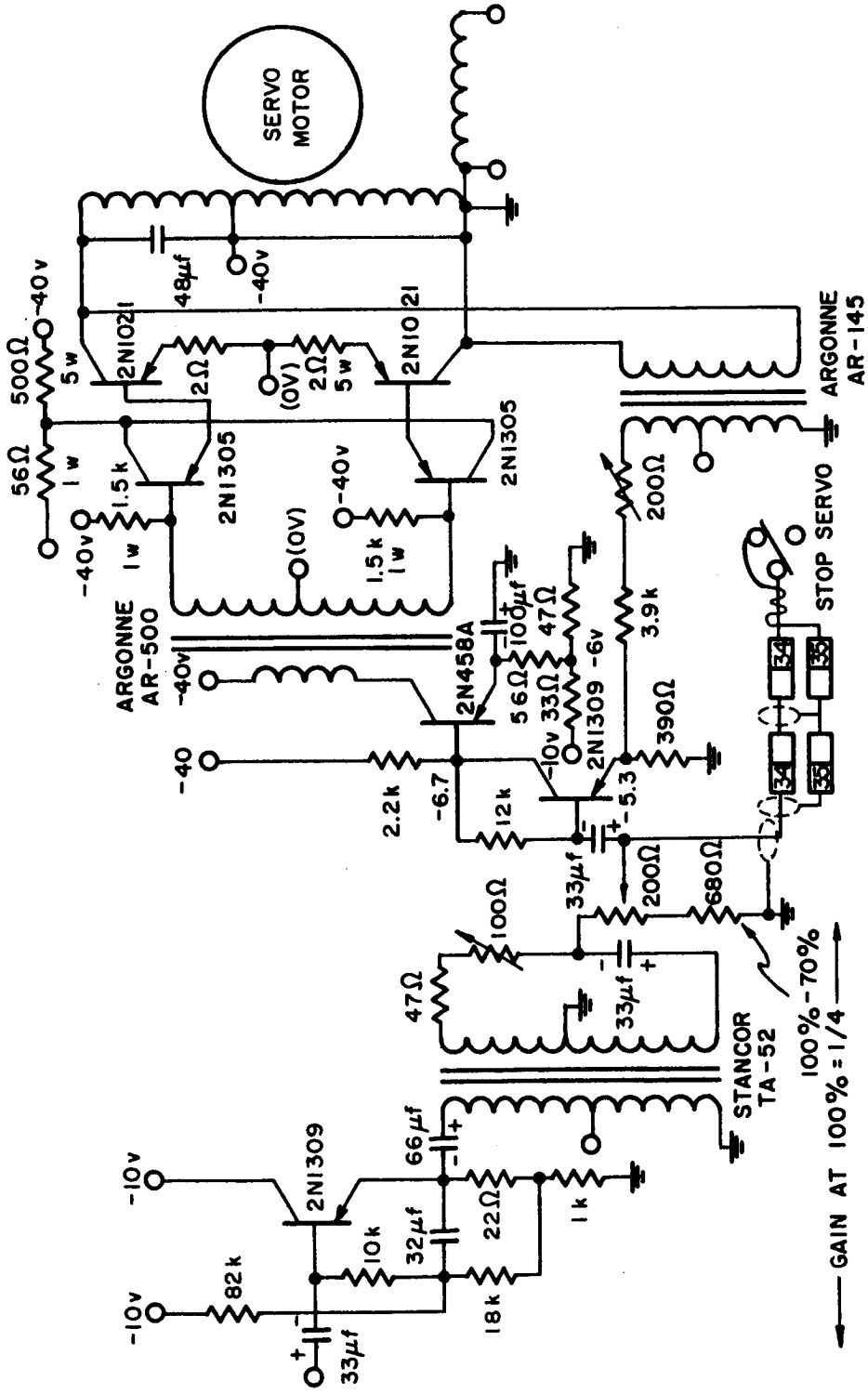


FIGURE 5-15 SERVOAMPLIFIER SCHEMATIC

The unit is of conventional design except for the fact that, even though it is an A-C amplifier, most stages are D-C coupled to minimize the number of energy storage elements. This technique provides a greater frequency response range and assures a stable design.

A motor with a -40V center-tapped high impedance winding was selected to avoid the use of a bulky output transformer. The maximum gain is 42. There is no noticeable phase shift between 30 cps and 90 cps at full power. The maximum voltage from the conveter is 1.92 volts which results in a maximum output voltage on the control phase of 80.6 volts at maximum gain. The theoretical undistorted maximum voltage is 80 volts. A STOP SERVO switch is provided in the control unit to short the servo-amplifier input when desired.

The first stage is an emitter follower so that the amplifier does not noticeably attenuate the signal from the digital-to-A-C converter. The transformer stage provides a variable phase shift network which does not vary the amplitude. It compensates for any phase shift in the amplifier and provides a 90^{o} phase shift between the control signal and fixed field voltage on the two-phase servo motor. This allows the fixed phase voltage to be taken directly from the line. The potentiometer provides the variable gain.

The second stage is a D-C amplifier with an unbypassed emitter resistance across which A-C feedback voltage is developed. The third stage is a typical driver stage to the Class B output. In this stage the emitter resistance is by-passed to increase gain.

The entire Class B stage is floating with its own power supply in order to meet the servomotor manufacturers' requirement that one leg of the control phase be at ground potential. To avoid cross-over distortion some Class A operation is provided by the base bias resistors. The next stage is an emitter follower stage. It seems to increase gain and to lower the total output impedance of the amplifier. A low output impedance is important to avoid single-phasing of the servomotor. The emitter resistance of the power output stage provides temperature compensation. The feedback transformer reconstructs the wave form and provides D-C power supply isolation. The large capacitor across the control phase tunes the motor to a low resonant frequency which further improves the low frequency response.

The open and closed-loop frequency responses are shown in Fig 5-16 Experimental waveforms are shown in Chapter VI.

Design of the Plant

Although the plant power output is small, the plant

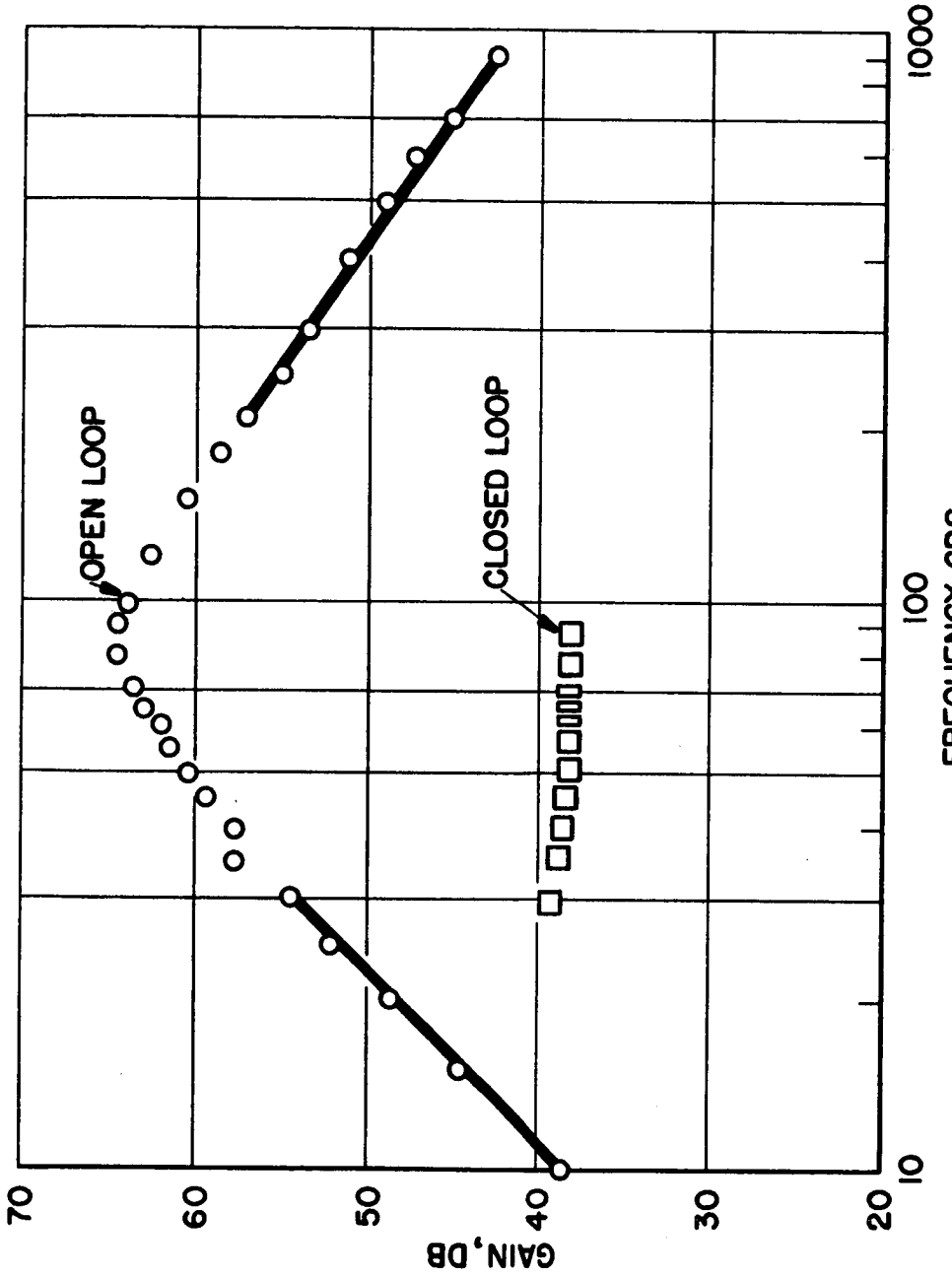


FIGURE 5-16 SERVOAMPLIFIER FREQUENCY RESPONSE

dynamics and feedback encoders are typical of large systems. The plant as designed represents a minimal system. Essentially only the feedback encoders are coupled to the load which is driven by the motor. In some systems[12] a tachometer is used to provide damping and to provide velocity information. The inertia of a tachometer is a large part of the total inertia of instrument servos and would reduce the dynamic performance. In this system, the compensator makes all the necessary calculations so that a tachometer is not necessary.

A block diagram of the digital servomechanism is shown in Fig 5-17. The range of the unit is 1/2 revolution of the coarse dial. To increase the resolution of the readout, it is presented on a coarse and fine dial. One-half turn of the coarse dial results in a number change of 2^{16}, or 65,536 units from the digital encoders. The coarse dial is divided into 50 parts. Each graduation of the coarse dial is equivalent to one turn of the fine dial. One turn of the fine dial is equal to 2621.5 units. The graduations of the fine dial are 2^{o}. Each 2^{o} graduation is equal to 14.5 units. A vernier is used to resolve the graduation down to 12 minutes of arc. Each 12 minute division of arc is represented by 1.45 units. Therefore, the digital resolution exceeds the analog resolution of the readout system. The analog-digital equivalents are summarized in Table 5-1.

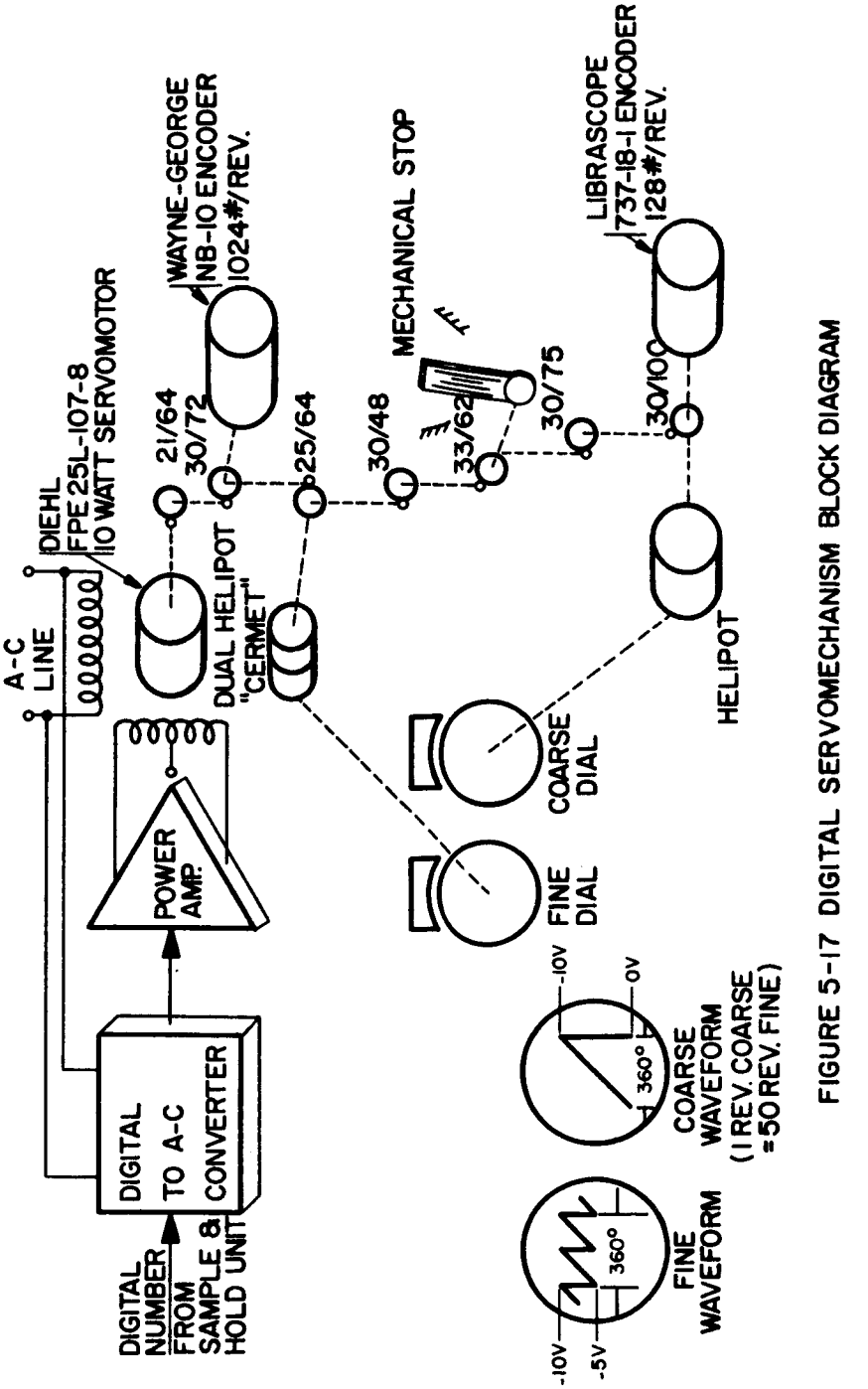


FIGURE 5-17 DIGITAL SERVOMECHANISM BLOCK DIAGRAM

Analog Quantity	Digital Quantity
1/2 Revolution of Coarse Dial	65, 536
1 Division of Coarse Dial	2, 621. 5
1 Revolution of Fine Dial	2, 621. 5
1 Division of Fine Dial , 2^{o}	14. 5
1 Division of Vernier, 12'	1. 45

Table 5-1 Analog and Digital Equivalents

To assist in obtaining dynamic measurements analog potentiometers are provided on the fine and coarse dials. A linear potentiometer cannot be electrically continuous. Consequently, two potentiometers (shifted 180^{o} with respect to each other) have been provided. The output waveform from each wiper is shown in Fig 5-18. By providing the diodes only the most negative voltage appears at the output - thus a continuous linear waveform is generated and the position within the open circuit range can be measured. The fine potentiometers generate two sawtooths per revolution of the fine dial. Thus 100 sawtooths of the fine potentiometer equal 1 sawtooth from the coarse potentiometer. The dynamic position of the servo can be obtained by simultaneously recording the output from both potentiometers.

The maximum speed of the motor is 3500 rpm (no load). Consequently, the speed of the first encoder approaches 475

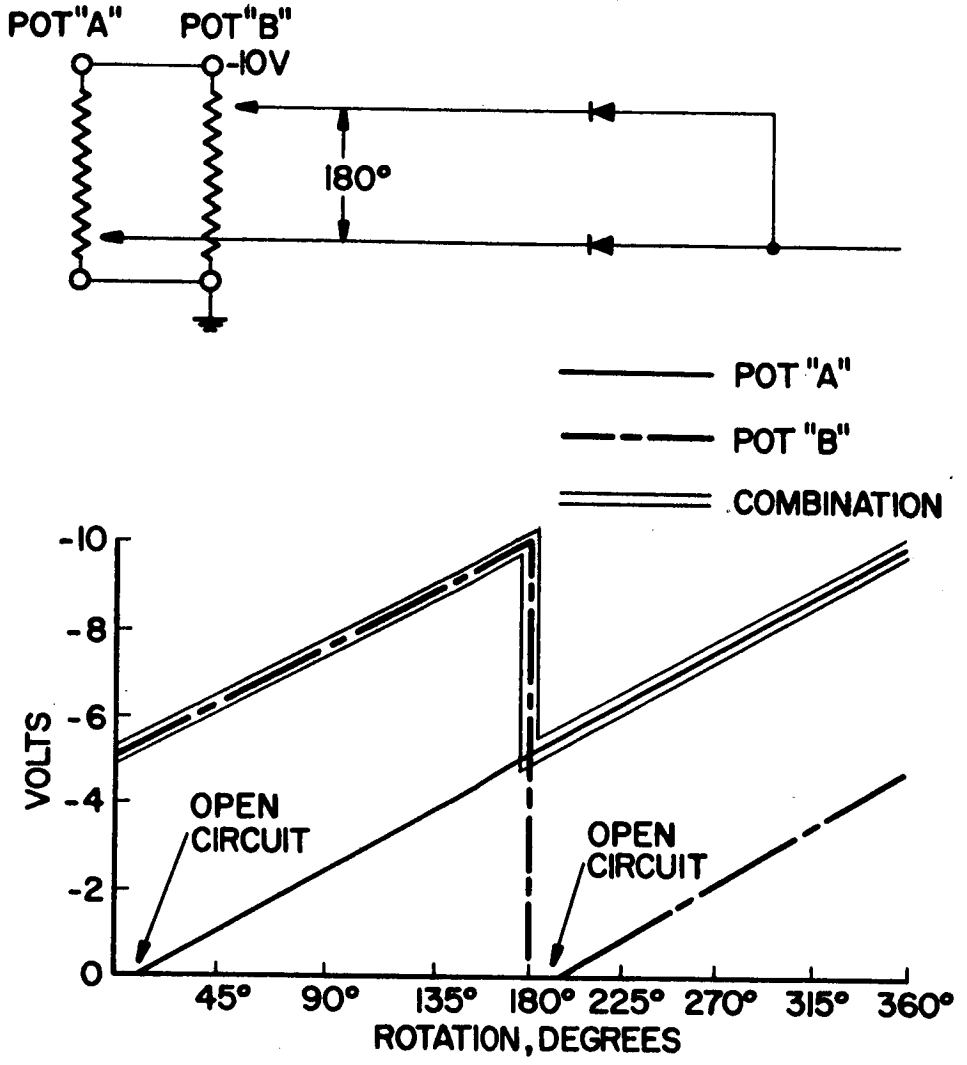


FIGURE 5-18 FINE ANALOG OUTPUT

rpm for the gear ratio shown. An optical encoder was chosen for this location since wiper bounce is eliminated. The coarse encoder speed is quite slow and wiper contacts are used there.

The fine analog potentiometer speed can approach 180 rpm. Consequently, a potentiometer with a "Cermet" resistance element was chosen. The use of this material eliminates the washboard ripple of wire resistance elements again reducing wiper bounce and increasing potentiometer life.

All gears are mounted on ball bearings, either in the unit or on the external components. This results in minimizing friction but, perhaps more important, the dimensions of the ball bearings are controlled so that the gear centers can be controlled. The gears are quality Precision 1. All gear centers were calculated for all tolerance variations and the initial portion of the gear train bored to a precision of 0.0002 inch. The gear bearing plates were bored in-line. There are no gear center adjustments, either to reduce backlash or to get out of adjustment later.

After assembly no backlash was discernible nor any high torque positions.

The complete digital servomechanism plant is shown in Fig 7-13. Notice that when the cover is on, the gear train is totally enclosed.

The function of the control system is to control the position of an output shaft of the plant. Accordingly the shaft position must be sensed and the information converted into a form compatible with the computer. The shaft changes its position continuously but the computer operates using numbers in a discrete form. Obviously, the control system cannot operate the shaft to a precision greater than the resolution of the least discrete unit.

There are two basic classes of analog-to-digital converters: incremental and absolute. An incremental encoder produces a change at the output for each discrete unit boundary traversed. To relate the present position with a reference, these changes must be totalized accounting for forward and backward motion. It should be noted that if a change is lost or an extraneous change counted, the result is in error. This source of error may be less serious in a slow system, but here we are compensating a high performance system for dynamics. An absolute analog-to-digital converter produces a unique code at its output for each discrete unit within its range. The unique code is referenced to an absolute position so that the present output does not depend upon its history. To make the encoders as compatible as possible with the computer, the natural binary code is retained.

There are three problems associated with the use of the natural binary code in encoders of high performance systems. One potential source of difficulty can be seen in Fig B-1by viewing the point at which the disc makes the transition from all ZEROES to all ONES. At the critical point, very small differences in disc markings or brush positions can result in some outputs being ONE while other channels are ZERO. This is obviously an incorrect reading. The requirement for positional accuracy is so great on such an encoder as to make its production impractical, if not impossible. Accordingly, both encoders used employ a "V-scan" system. The least significant channel employs a single brush. All other channels employ two brushes which are spaced to the left and right of the least significant channel brush, the spacing increasing from channel to channel toward the more significant channels. The increasing spacing of the brushes in the direction of the more significant tracks is the reason for other "V-scan" title. Logical circuits determine which brush will be read at any particular time. Once the "V-scan" system has examined the least significant bit and determined whether it is a ONE or a ZERO, it will always select a brush that is so located that it is either fully ON or fully OFF. Thus, only the transition point of the first channel has any significant effect on system

operation and in this channel, only by a single discrete unit.

The logic of the "V-scan" system and the features of the particular encoders employed are given in Appendix B.

There is a second potential problem with the encoder in this high performance system, i.e,, the possibility of erroneous readout due to bouncing brushes at high speed. With full speed on the motor (3500 rpm) the fine encoder will rotate at 475 rpm. Accordingly, an optical unit was selected for the fine encoder as discussed earlier. The coarse encoder turns slowly even with full speed from the motor so brush contacts are used there.

The principle of operation of the optical encoder is shown in Fig 5-19. The encoder consists of a glass disc encoded in natural binary by an array of opaque and transparent segments. An incandescent lamp unit illuminates a radius of the code disc and a photosensitive detector assembly detects presence or absence of illumination. Hence, the encoder is of the non-contacting type.

There is a third potential problem for this high-performance system associated with the use of the "V-scan" system. The serial nature of the brush selection requires a finite time period to go from the least significant digit to the most significant digit. An example is the transition from all ONES to all

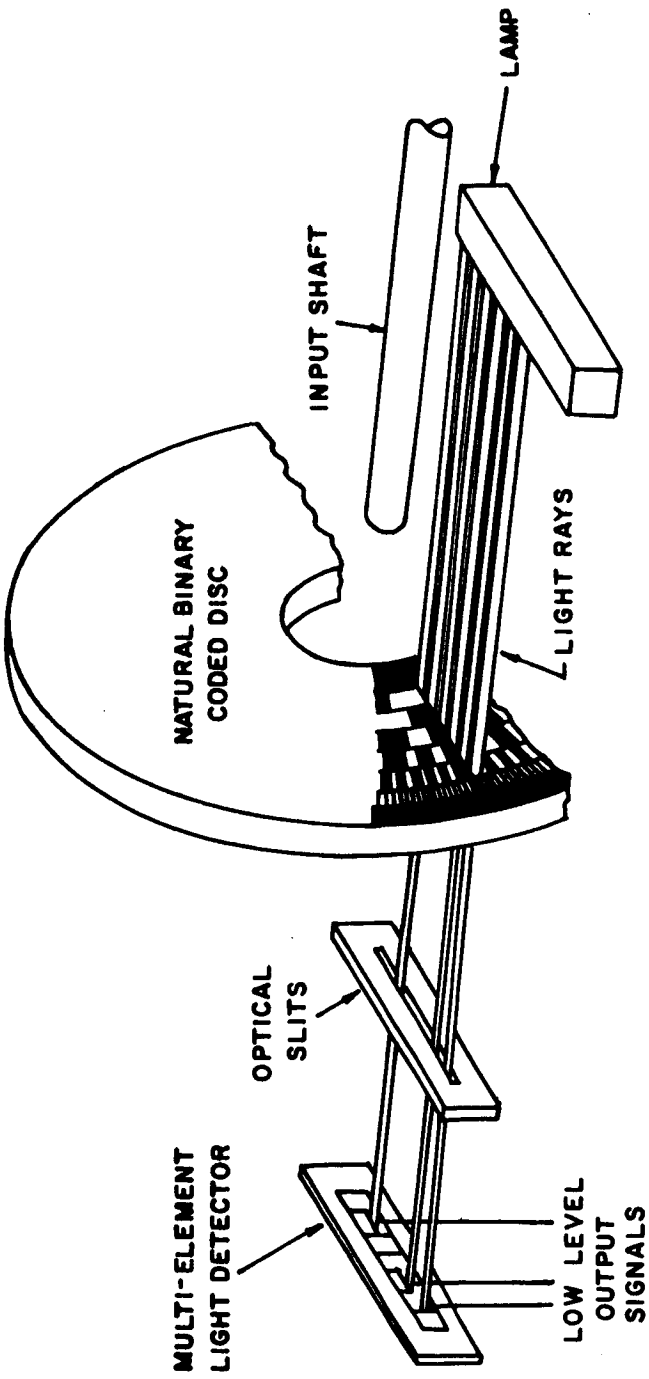


FIGURE 5-19 OPTICAL ENCODER

ZEROES which starts off at the least significant bit and then propogates toward the most significant bit one channel at a time. Each channel changes from a brush reading a ONE to a brush reading a ZERO. An erroneous readout would occur if we sampled the output during such a transition. Accordingly. a control signal locks the least significant digit in its present position. 50μ sec. before the desired readout time so that all channels are settled down during readout. At full motor speed the maximum change which can occur during this time is one-half a least significant digit. This 50μ sec control signal was made an integral part of the system logic. (See Clock Timing, Table 4-2C(T0I8)).

Proper logical circuitry and gear ratio are required to couple the brush encoder to the optical encoder. The brush encoder's least significant digit brush normally switches the V-brush logic of the more significant digits. In order to achieve unambiguous readout from the coupled encoders it is necessary to continue the basic V-brush logic through the coupling, i.e., one of the brushes of the least significant track of the brush encoder should be chosen by logical circuitry controlled by the sensors of the most significant digit of the optical encoder. Thus, the least significant digit track of the brush encoder must have two brushes on it.

This means that the track which is normally the least significant digit and has only one brush contacting it must be ignored. Instead of the brush encoder having a 2^7 range, in this application it has a useful range of only 2^6. The gear ratio is chosen so that one revolution of the brush encoder requires 2^6 revolutions of the optical encoder. Hence, the gear ratio between the encoders must be 2^6 (64:1).

The logical circuitry coupling the two encoders is given in Fig (5-20). Notice that pin (1) is controlled by the output of the 2^9 track of the optical encoder through the NOR-1 gate. The divider network at the output of the NOR-1 has been changed and pin O has been disconnected. When used in a normal application pin O controls the logical circuitry.

This basic technique may be applied repeatedly to achieve any desired range. The worth of the least significant digit of the optical encoder ultimately depends upon the backlash, accuracy and wearability of the gear train.

The dynamic response of the plant including the servoamplifier is given later in Chapter VII.

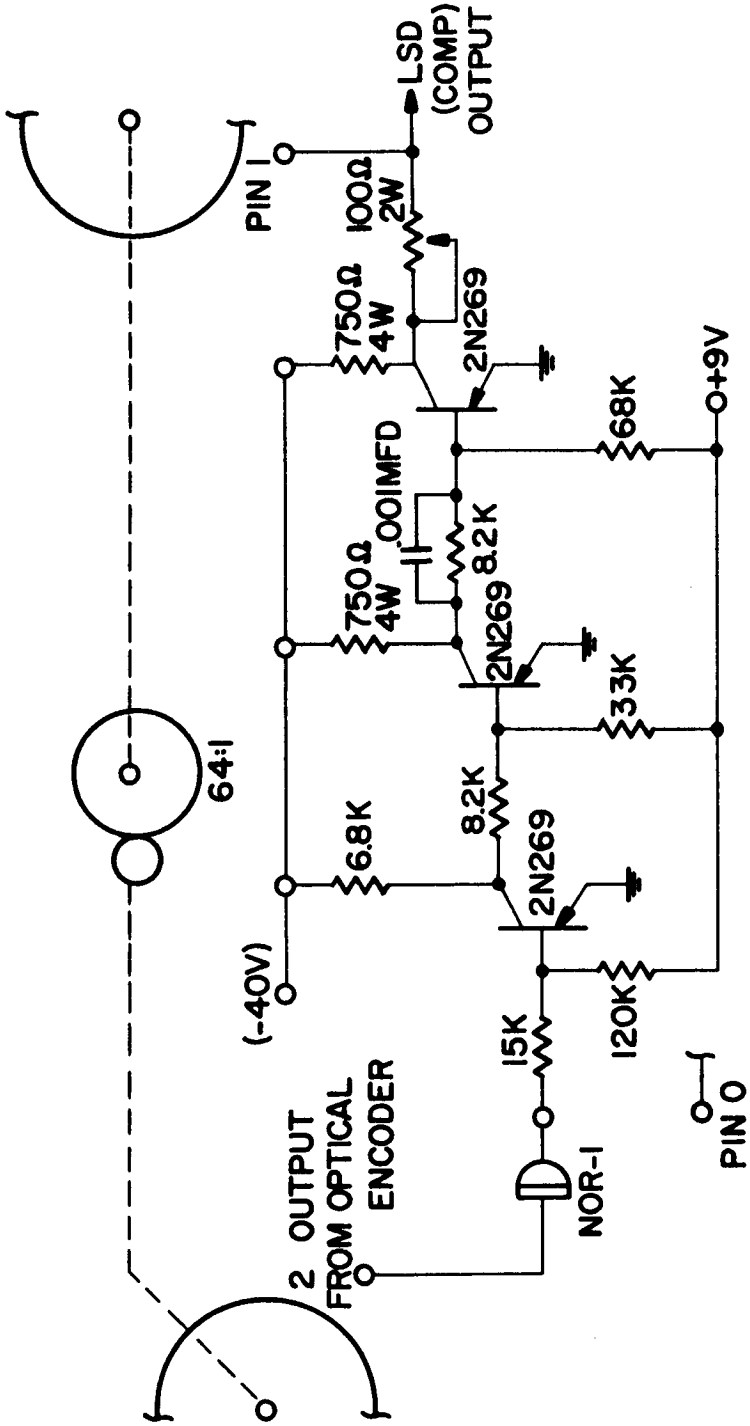


FIGURE 5-20 OPTICAL TO BRUSH ENCODER COUPLING

VI DESIGN OF THE AUXILIARY EQUIPMENT

It is not sufficient to design only the components of the compensator and plant. Some provision must be made to put efficiency and facility into the testing and operating program. The purpose of the Control Unit is to meet this need.

Design of the Control Unit

Some means must be provided to insert the proper constant coefficients into their respective integrator positions. As discussed earlier, the clock track divides the diameter of the drum into radial segments. The length of the drum is then divided into tracks with one track being the area which passes under a head each revolution. The drum surface is shown in Fig 6-0. The clock and tach read heads are shown. To accommodate the remainder delay timing (see Fig 4-9) the read-write heads are spaced precisely 106 clock bits apart (nominally 1.11 inch). The point here is that the drum surface is divided into segments (one is shown shaded in Fig 6-0). These segments each possess an "address" which indicates their position on the drum surface. We need to be able to read or write from any address. Also to gain speed in the computations, the digits of an entire word can be written simultaneously.

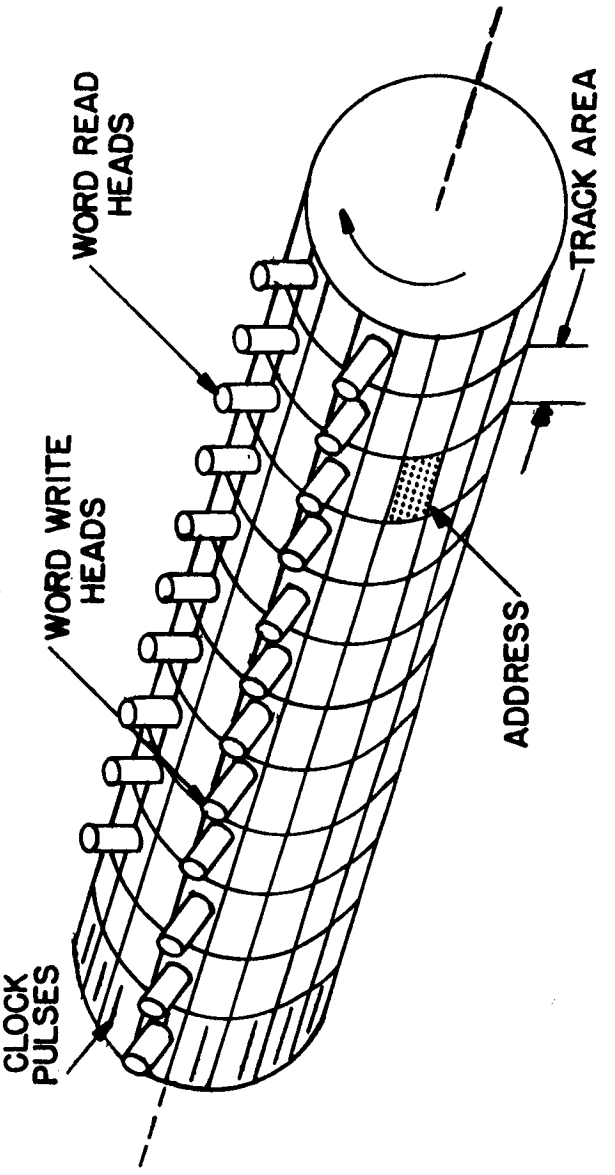


FIGURE 6-0 ADDRESS AND READ-WRITE HEAD LOCATIONS

Design of the Address Circuit

The design problem is to know in time when the desired address is under either the read or write heads. Since the clock counter has in it the radial portion of the address, we use a set of switches and an identity circuit, to give us a pulse when the radial address and switch positions are in correspondence. The circuitry is given in Fig 6-2 and the Address switches can be viewed in Fig 7-7. The switches correspond to Integrator Number and Integrator Sector.

The inputs to the i^{th} stage are $\overline{I}$ and i.
The diode network forms an AND gate and the resistor-transistor circuit a NOR gate. The truth table is

I	i	Identify
0	0	1
0	1	0
1	0	0
1	1	1

Fig 6-1 Identity Truth Table

From the truth table, an

$$\text{Identity} = \overline{I}i + \overline{I}\overline{i} = \overline{(\overline{I}i)\ (\overline{\overline{I}\overline{i}})} = \overline{(\overline{I}+\overline{i})\ (I+i)}$$
$$= \overline{\overline{i}\ I+i\ \overline{I}} \quad \overline{= \overline{I}\ i+\ (\overline{\overline{I}+i})} \qquad (6\text{-}1)$$

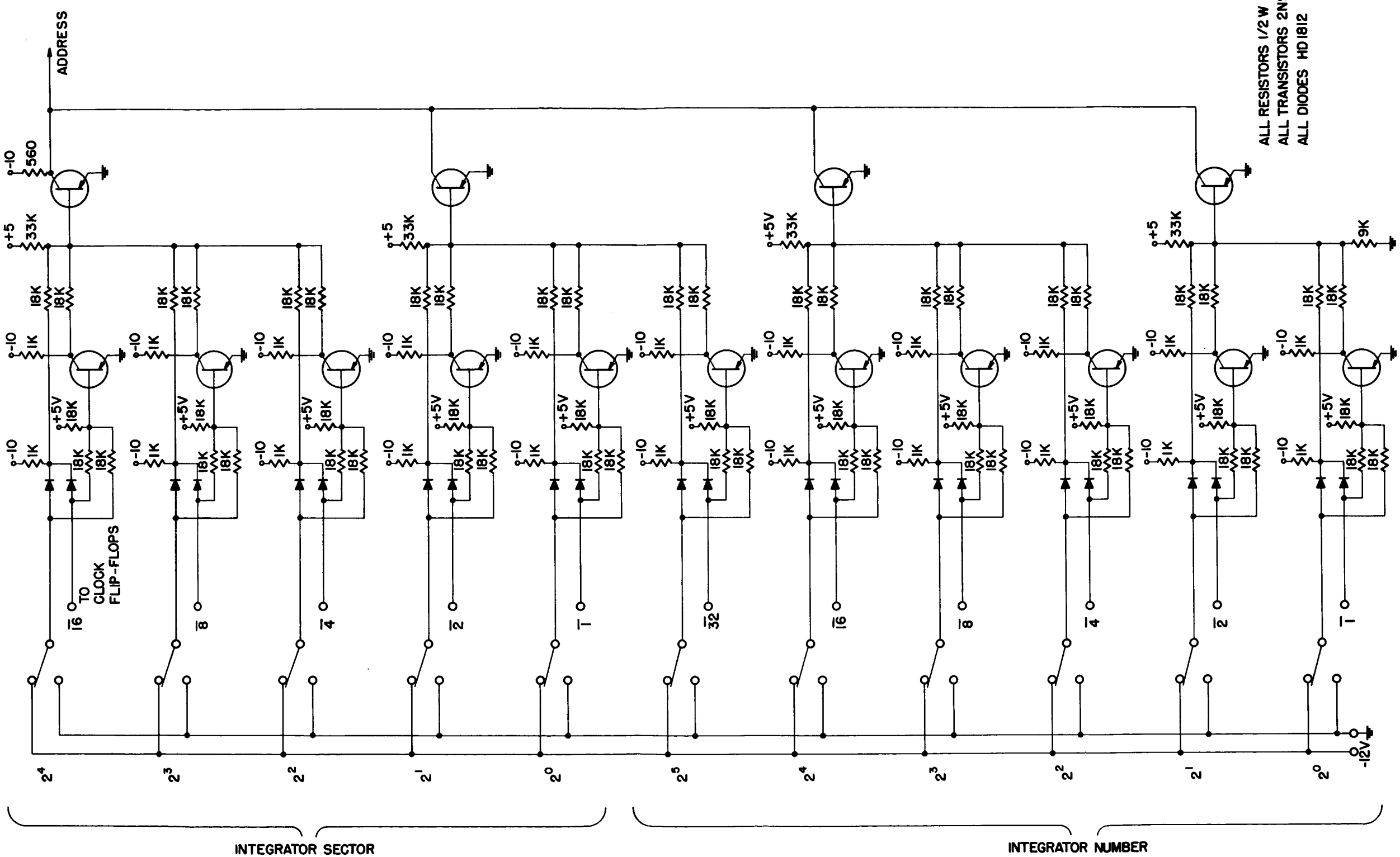


FIGURE 6-2 ADDRESS SCHEMATIC

An identity formed by the and stages is

$$(I\,i + \overline{I}\,\overline{i})(J_j + \overline{J}_{\overline{j}}) = \overline{(I\,i + \overline{I}\,\overline{i})} + \overline{(J_j + \overline{J}_{\overline{j}})} = \overline{(\overline{I} + \overline{i})(I+i)} + \overline{(\overline{J}+_{\overline{j}})(J+_j)}$$

$$= \overline{\overline{I}\,i + \overline{i}I} + \overline{\overline{J}_j + {}_{\overline{j}}J} = \overline{\overline{I}\,i + \overline{(\overline{I}+i)}} + \overline{\overline{J}_j + \overline{(\overline{J}+_j)}} \quad (6\text{-}2)$$

and so on. To complete the identity circuit the output from all AND gates and NOR gates are NOR-gated together to form the address.

Design of the Word-to-be-Written Circuit

To write the coefficients into their respective addresses we need a Word-to-be-Written circuit. The bits of the word are entered into the control unit by means of the switches and a circuit is required to write the word in the correct address. The switches can be viewed in Fig 7-7. The circuit is shown in Fig (6-3). In order to write a word on the drum, the write amplifier must be enabled in addition to providing a pulse at the read amplifier input. (See Appendix C). For this reason, each bit of the word has two gates associated with it, the write amplifier input and the write amplifier enable. The word must be written in an address without disturbing the word in an adjacent address. It is unnecessary for the word to be written on the drum more than once, and repeated unnecessary writing might cause unnecessary smearing. For this reason, all gates

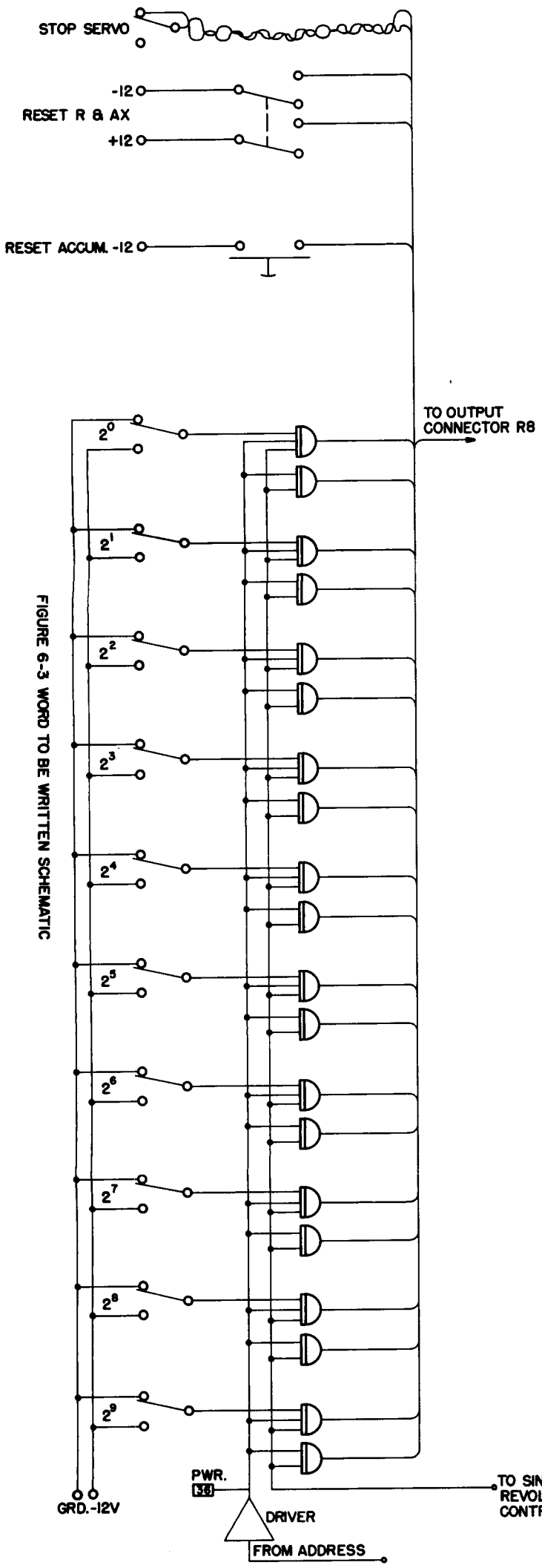


FIGURE 6-3 WORD TO BE WRITTEN SCHEMATIC

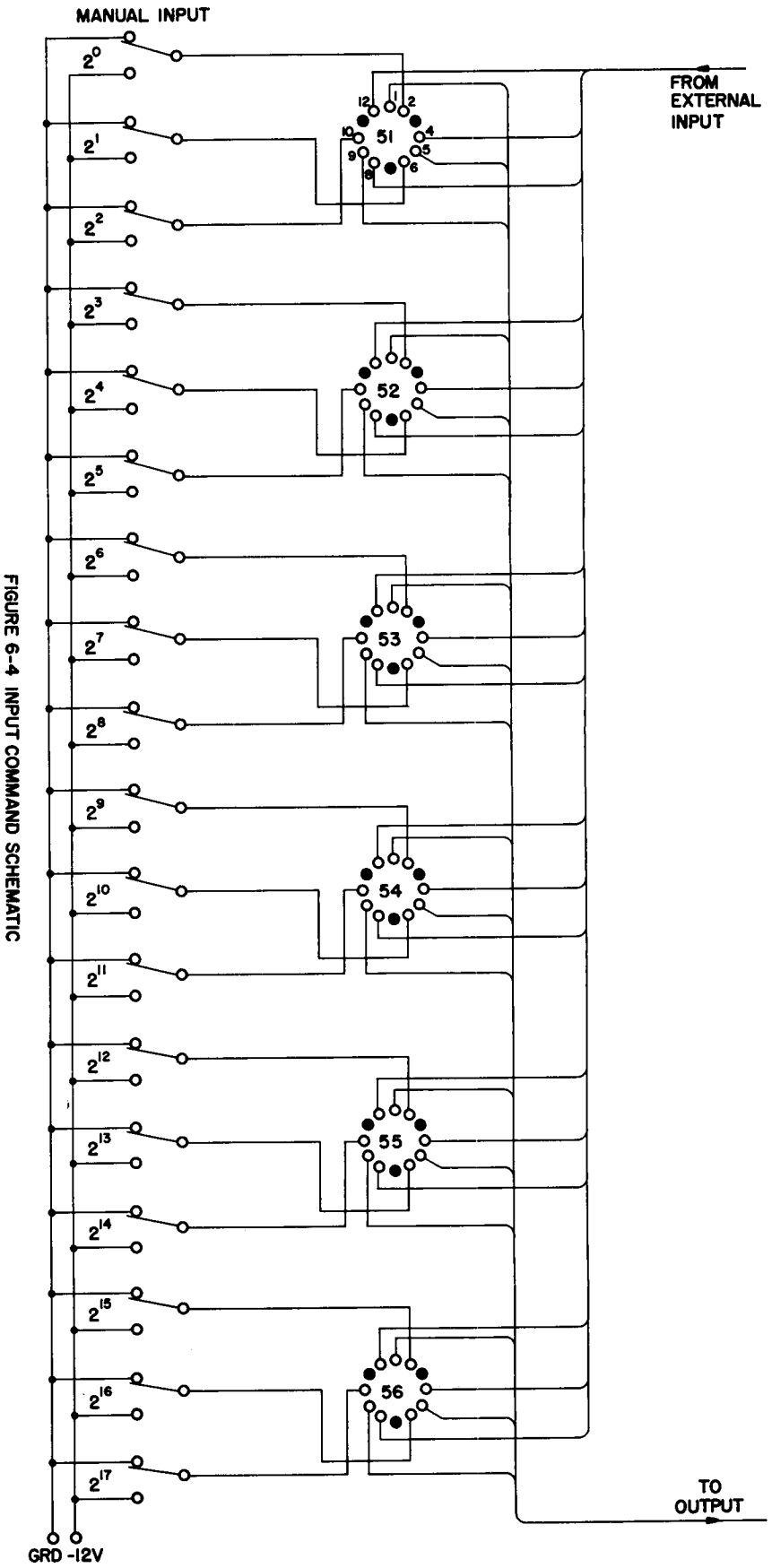


FIGURE 6-4 INPUT COMMAND SCHEMATIC

SHADED SWITCH POSITIONS ARE GROUND POTENTIAL

are ANDED with another line which is TRUE for only a single drum revolution. The gates of the Word to be Written circuit are also shown with the write amplifiers in Fig (5-10).

Design of the Single Drum-Revolution Circuit

The clock controls all operations in the compensator. When the clock stops the compensator stops. Therefore, the design problem to obtain a single drum-revolution control circuit is to provide a control which allows the clock to operate for only a single cycle.

The switches on the control unit are used in conjunction with the circuit given in Fig (6-5). These are the START-PREPARE switch and the OPERATION switch.

With the switch in PREPARE, the emitter of the FF transistor is open and -12v is applied to the gate stopping the clock. Any switches can be changed without effecting the system operation when the switch is in the PREPARE position. When the OPERATION switch is in HOLD, the clock is again stopped. When the OPERATION switch is in the CONTINUOUS position, that leg of the gate is at ground potential and if the operation is not over-ridden by another control the clock will run continuously. The clock is under the control of the single drum-revolution circuit when the OPERATION switch is in the SINGLE

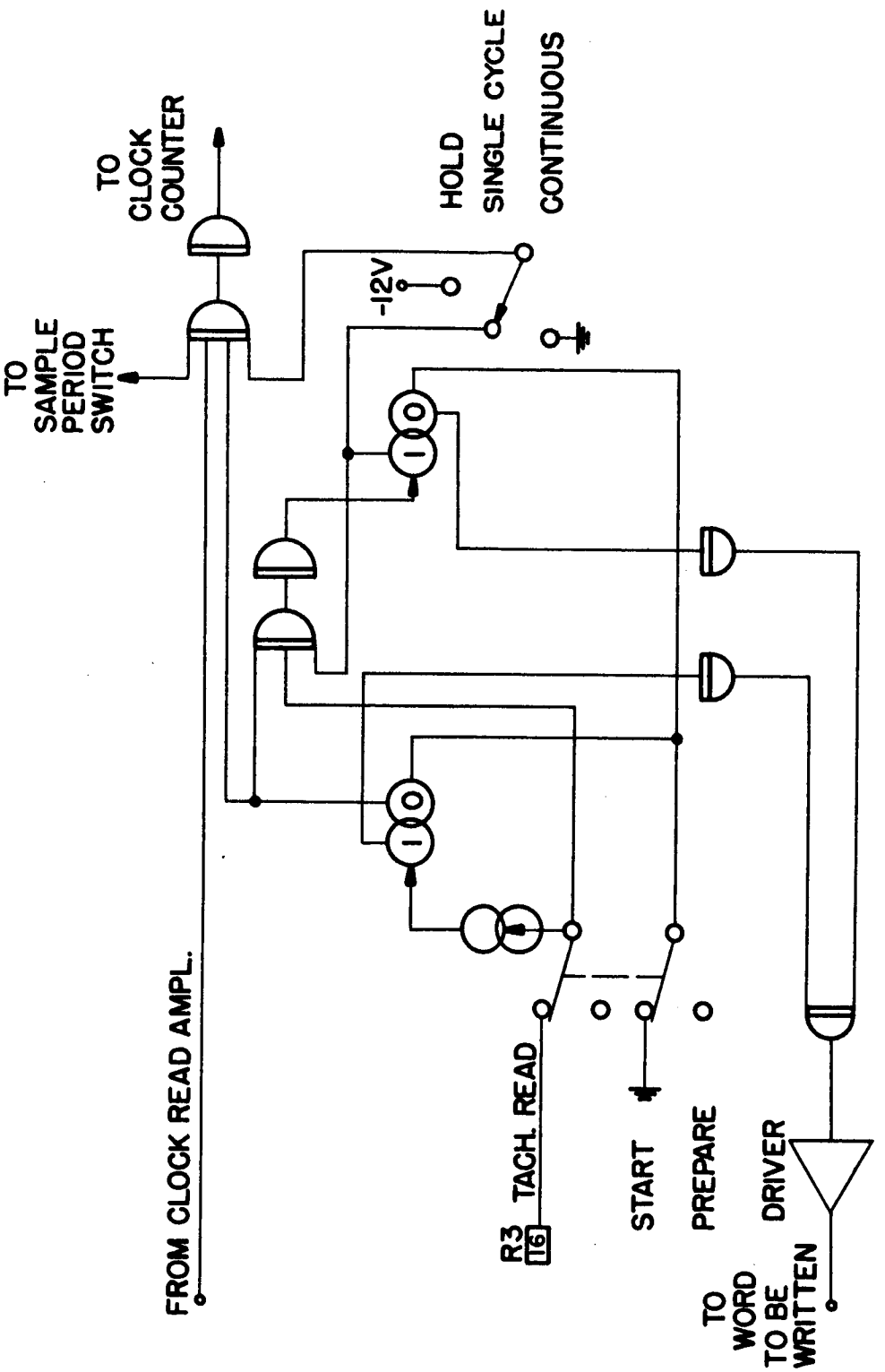


FIGURE 6-5 SINGLE DRUM-REVOLUTION CONTROL LOGIC

CYCLE position.

When the switch is placed in the START position, the clock is still stopped by the FF on the left in Fig (6-5). The output of the right FF is at ground. A signal is blocked to the driver circuit by the AND gate. When the first tach pulse arrives indicating the beginning of a cycle, it first raises the center of the 3-input AND gate to ground, then resets the left FF. Due to the one-shot multivibrator delay, the tach pulse is gone before the FF is reset. When the FF resets, 1) the 3-input AND gate does not conduct, 2) the clock starts and 3) the driver conducts allowing the Word-to-be-Written circuit to operate when the correct address is reached. After one revolution, a second tach pulse arrives which now causes the 3-input AND gate to conduct which resets the right FF which in turn stops the clock.

Thus, the Word-to-be-Written circuit was enabled for a single drum revolution.

Design of Reset Features

When using the compensator there are times when reset features are advantageous. There are three RESET switches on the control unit SERVO, ACCUMULATOR and REMAINDER ΔX

The SERVO switch grounds the input to the servo-amplifier as discussed previously and shown in Figs (5-15) and (6-3).

The ACCUMULATOR switch, when depressed, resets the accumulator FF register.

The REMAINDER & ΔX switch serves to clear the integrators. We do not want to be able to clear the coefficients of each integrator from the drum easily, since these numbers are permanent for any given plant and desired performance. When the REMAINDER & ΔX switch is depressed a relay mounted in the rear of the MEMORY UNIT (see Fig 7-2) overrides the enable and input lines to the write amplifiers and writes all ZEROES in all remainder and ΔX addresses.

Design of the Sample Period Control

For an extensive experimental program a means is provided to change the sample period of the compensator. The SAMPLE PERIOD control circuit is shown with the clock circuit in Fig 5-12. The tach pulses go into a 4-bit counter, with reset of the counter being under the control of the START-PREPARE switch. When the SAMPLE PERIOD switch is in the 1 position the period is 0.018 milli sec. When it is in the 0.5 and 0.25 positions, the periods are 0.036 and 0.072 millisec.,

respectively. This is accomplished by allowing the clock to operate 1/2 the time or 1/4 the time.

Design of the Display

The purpose of the DISPLAY is to present a visual display of key information processing junctions within the compensator. It is particularly useful for trouble shooting. The junctions which are available on the DISPLAY are the contents of: the CONSTANT register, the REMAINDER register; the ΔX register; the REMAINDER DELAY register and the inputs of the WRITE AMPLIFIERS; and the ACCUMULATOR register and the outputs of the READ AMPLIFIERS. These are available by placing the DISPLAY switch in the C, R, ΔX, RD & WA or ACCUM & RA positions, respectively.

The information can be displayed on a continuous basis or the information corresponding to one of the DISPLAY switch positions can be selected from the complete cycle by means of the ADDRESS circuitry. For example, to view the ΔX commands of all integrators in sequence one display switch is placed in the ΔX position and the other in the CONTINUOUS position. With the SAMPLE PERIOD in the 1 position, new information will be displayed every 384μ sec. (32x 12). However, to view the ΔX

commands of integrator 5 only in sequence, one display switch is placed in the ΔX position, the other is placed in the ADDRESS position, and the ADDRESS switches are set to INTEGRATOR number 000101 (5) and the INTEGRATOR SECTOR to 00101 (5). (See Table 4-2). With the SAMPLE PERIOD in the 1 position, new information will be displayed every 18 millisec.

Since the time intervals between the display of new information are too short for the naked eye except when the OPERATION switch is in SINGLE CYCLE, a digital to d-c voltage ladder [14] is used to provide an analog voltage proportional to these quantities. The output of the voltage ladder is made available for use with a recorder at the ANALOG test points. Thus, the key information processing junctions of the compensator can be recorded versus time.

Design of the Program Control

The logic of the compensator is designed to operate from either one of two stored programs. When the PROGRAM switch is in the 1 position, the compensator is under the control of program 1. When the PROGRAM switch is in the 2 position the compensator is under the control of program 2.

The effect of changing the switch position can be seen in the clock circuit, Fig (5-12).

The clock pulse is changed so that the command, read constant, is moved forward or backward one address position on the drum. Thus a separate set of coefficients can be stored in each of the two constant coefficient addresses.

This feature provides great flexibility in the use of the compensator because in conjunction with the input command control to be described next the compensator can be operated as a remote computer.

Design of the Input Command

The INPUT COMMAND control provides input command information to the plant. The input command is a digital number which has a different meaning to the plant depending upon the compensator program. For example, if the compensator is programmed for the plant to be a position servo, then the INPUT COMMAND represents a position command. If the compensator is programmed for the plant to be a velocity servo, then the INPUT COMMAND represents a rate command.

There are three positions for the INPUT COMMAND switch; MANUAL, ZERO and EXTERNAL. In MANUAL the INPUT command corresponds to a number generated by the row of switches. In ZERO, the INPUT COMMAND is zero. By switching from one position to the other step function commands can be generated. In EXTERNAL,

the contents of an external register, which may be under the control of another computer, would be the input command to the plant.

The input command schematic is shown in Fig 6-4. The manual input switches and control can be viewed in Fig (7-7).

Operation as a Remote Control Computer

By using the PROGRAM and EXTERNAL INPUT COMMAND controls, it is possible for the compensator to operate remotely under the direction of a master computer.

Notice, that the master computer need only provide input commands every 18 milliseconds to change the input command at its maximum rate. The stored internal program of the compensator would make all the necessary calculations on a microsecond level. The master computer could change the input command whenever a process being controlled began a new phase. The master computer could change the compensator program to achieve totally different performance from the same plant during different phases of a process.

Design of the Power Supplies

There are many different power supplies required in the compensator since it was necessary to incorporate available

commercial components into the system. The servomotor dictated the use of -40V supplies. The optical encoder dictated the use of +12V, -12V, and floating 5V supplies. The brushencoder requires -40V and +9V supplies. The logic circuits require -12V and +6V supplies. The memory unit read and write amplifiers require -15V, -10V and +5 V supplies. Since the memory unit is to become a permanent part of the digital simulator - commercial supplies were purchased for it. The regulation of these supplies is better than any of the others so the arithmetic unit circuitry was designed to use these supplies.

Since all the supplies are similar, only the -40V design will be described.[15] The rectifiers are arranged in a full-wave bridge to obtain higher transformer utilization and a high ripple frequency. The capacitor acts as a filter. The 2N250 transistor serves as a series regulator resistance. The output voltage is sampled at the potentiometer and applied to the base of the 2N1309 which serves to compare the output with the reference voltage provided by the reverse biased Zener diode. Bias current for the Zener diode is obtained from the output through the 3.9K resistor. Any error from the comparator is applied to the base of the 2N1309 in compound connection with the series regulator. A compound

connection is used to lessen the base drive required to maintain the load current. A collector resistor is used in the compound connected transistor which serves to limit short circuit current.

If the collector circuit is connected directly to the output any remaining variations in the output (such as ripple) will be amplified by the series regulator. The 270Ω resistor and the 1N708 Zener diode form a preregulator for the collector circuit of the comparator and further reduces output ripple.

The component values for the other supplies are shown in their respective circuit diagrams, Figs 6-6 to 6-8.

Since the +9V supply used in the brush encoder is less critical a simple full-wave rectifier and emitter follower voltage regulator is used as shown in Fig (6-9).

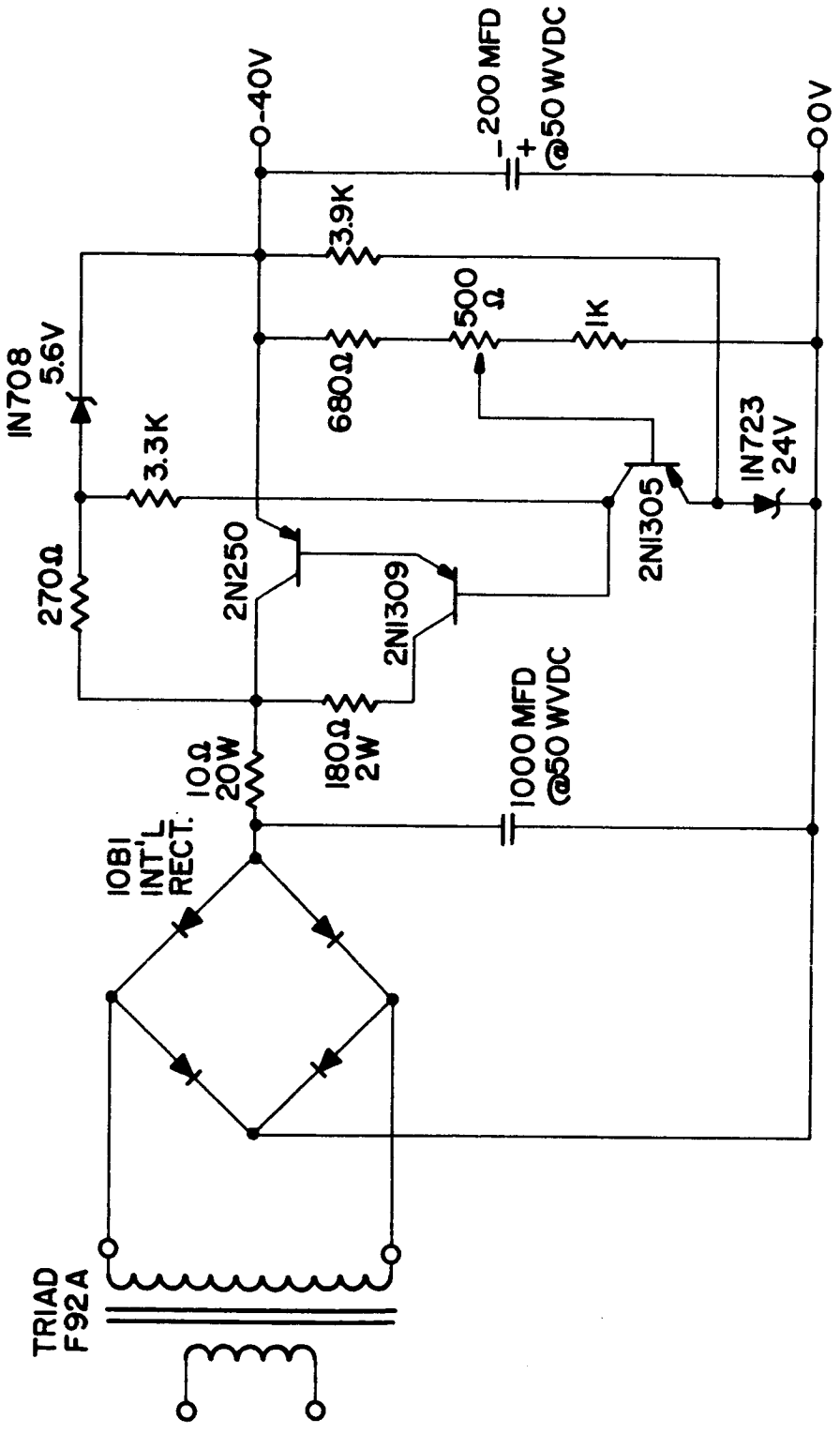


FIGURE 6-6 -40 V POWER SUPPLY SCHEMATIC

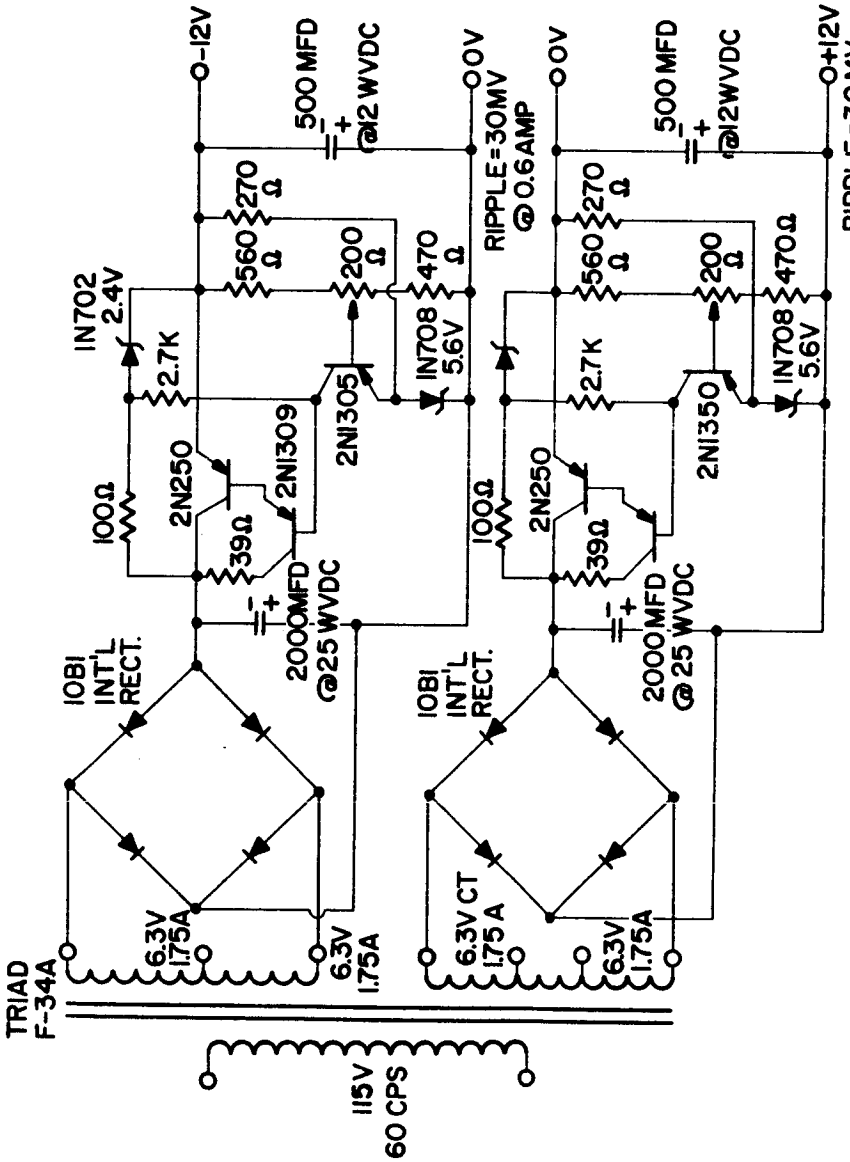


FIGURE 6-7 +12 AND -12V POWER SUPPLY SCHEMATICS

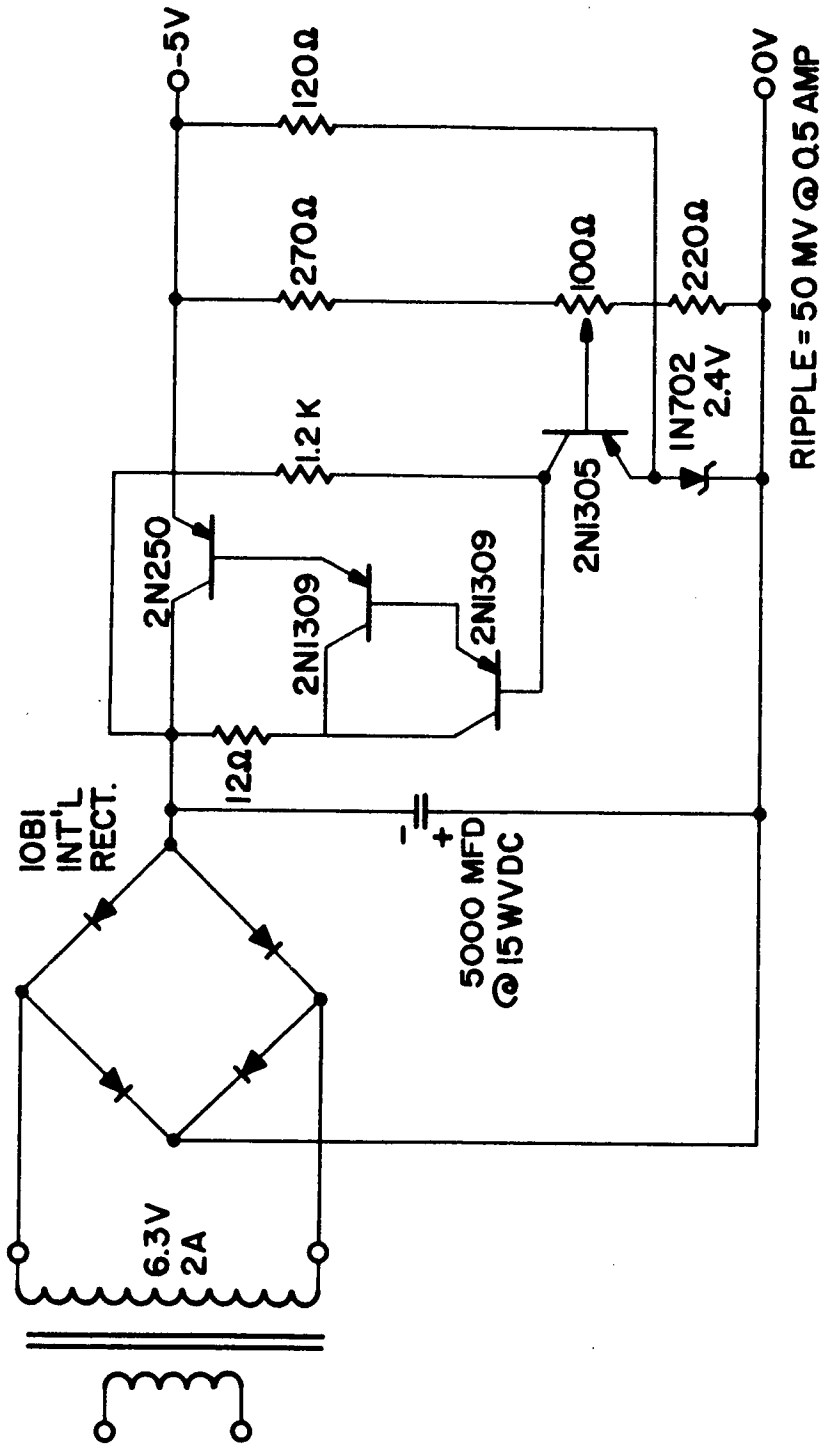


FIGURE 6-8 -5V POWER SUPPLY SCHEMATIC

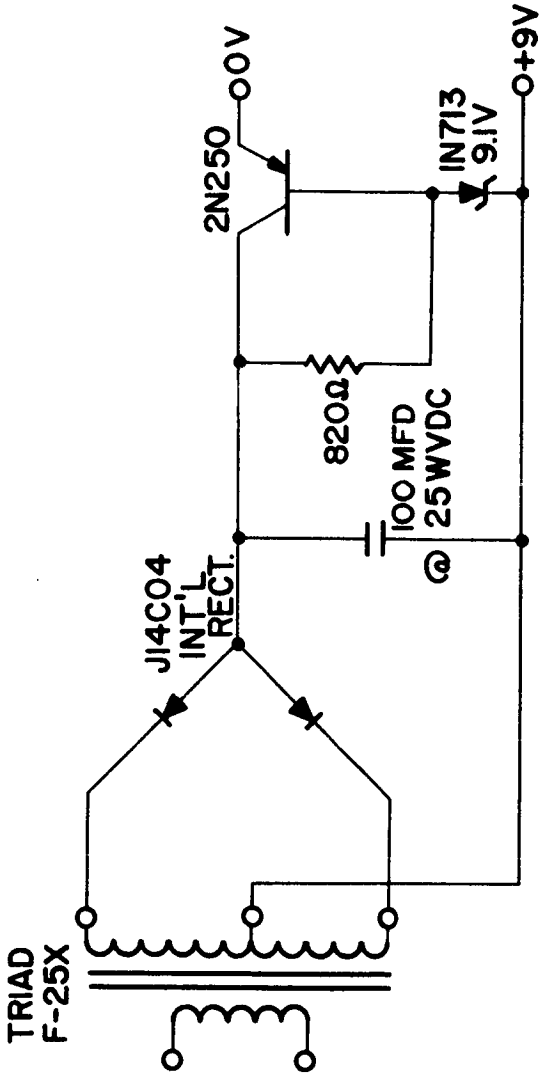


FIGURE 6-9 +9V POWER SUPPLY SCHEMATIC

VII EXPERIMENTAL RESULTS

The digital compensator and simulated plant are shown in Fig (7-1). All the registers and associated logic circuits were wired using the logic synthesizer available in the Numerical Control Laboratory. The logic synthesizer is shown on the right with the simulated plant located on top. The custom circuits required for the digital compensator are shown on the left.

Memory Unit

The memory unit consists of the read-write electronics mounted in the lower drawer and a standard magnetic drum.

The memory unit was constructed to be a permanent addition to the logic synthesizer. The construction details of the memory unit electronics are shown in Fig (7-2). The bottom cover and internal wiring of the other units are similar to those of the memory unit. The write amplifier is shown in Fig (7-3). The read amplifier is shown in Fig (7-4). The commercial magnetic drum is shown in Fig (7-5). The test jacks on the front panel of the drawer allow access to the waveforms required to adjust the read amplifiers. An amplifier test unit is shown in Fig (7-6). The theory of operation and description of the waveforms are given in Appendix C.

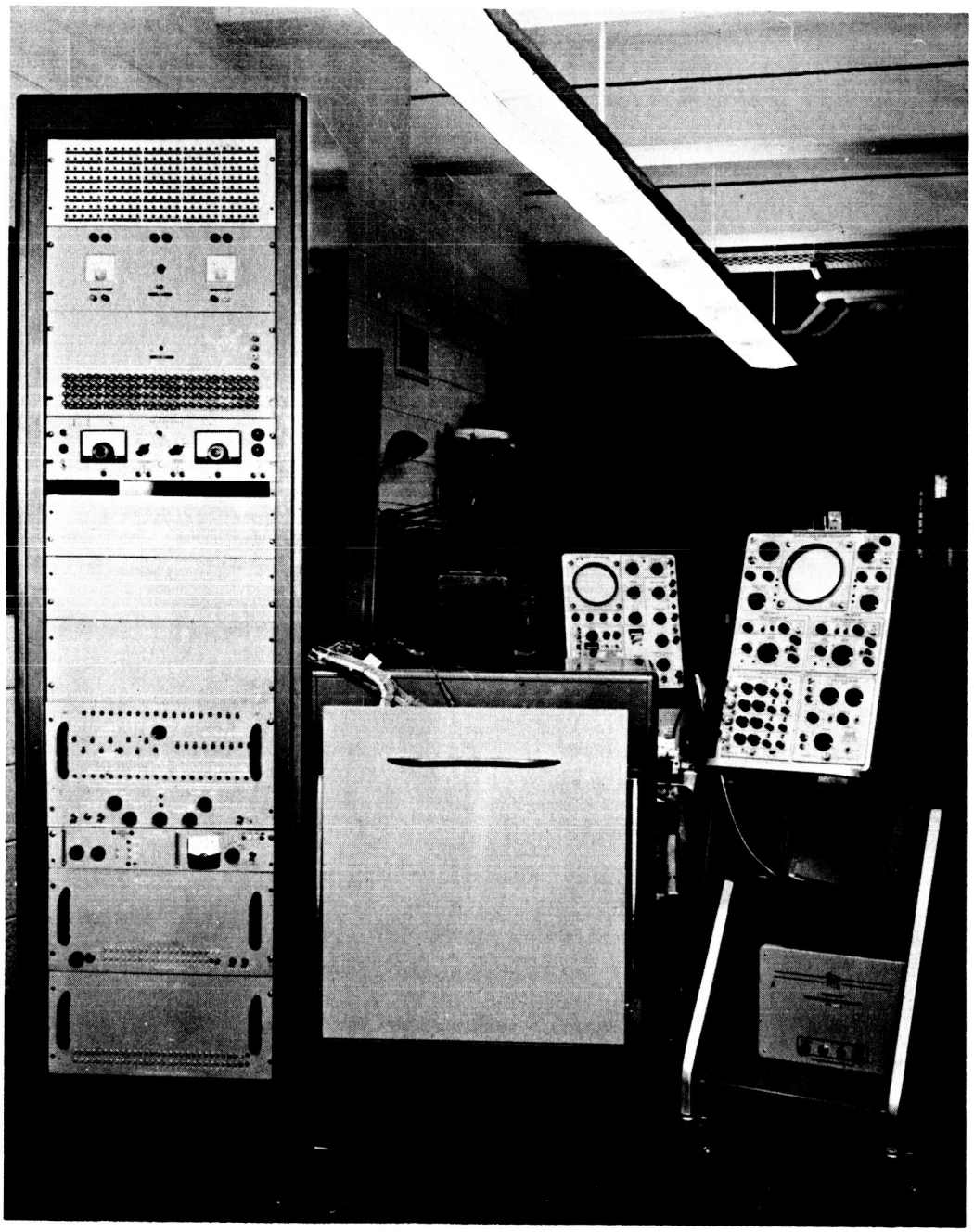


FIGURE 7-1 DIGITAL COMPENSATOR & PLANT SIMULATOR

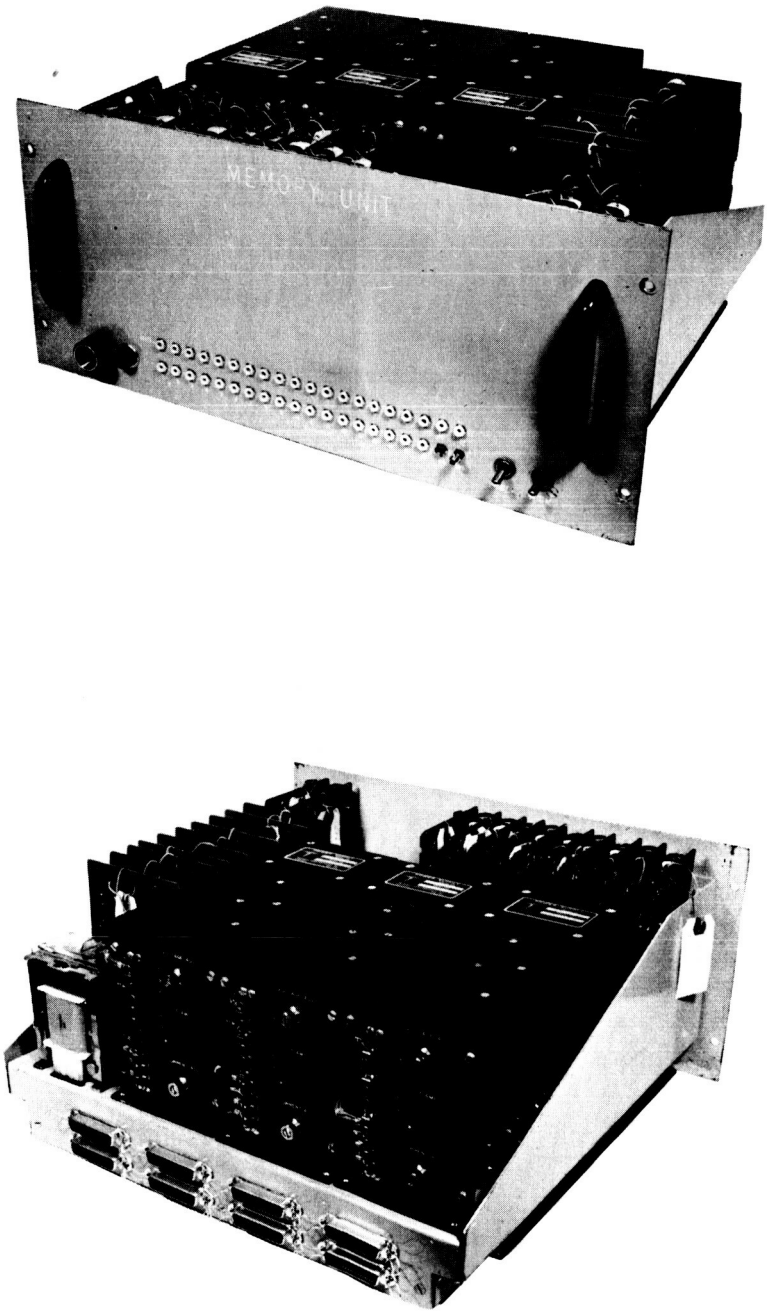
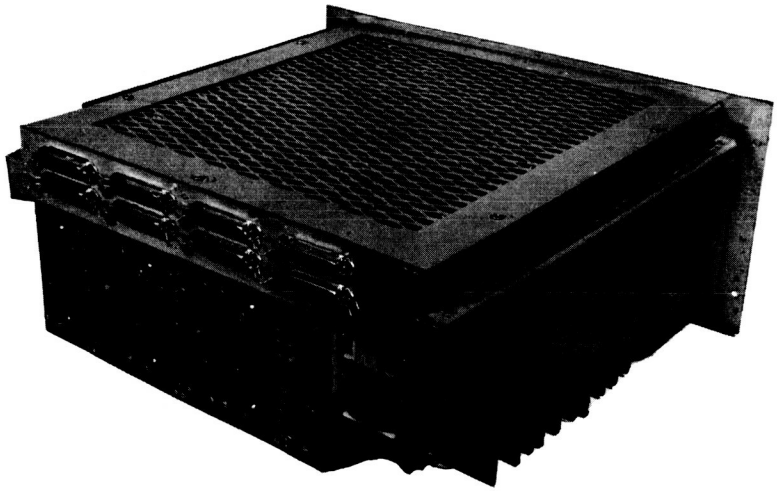


FIGURE 7-2 MEMORY UNIT ELECTRONICS



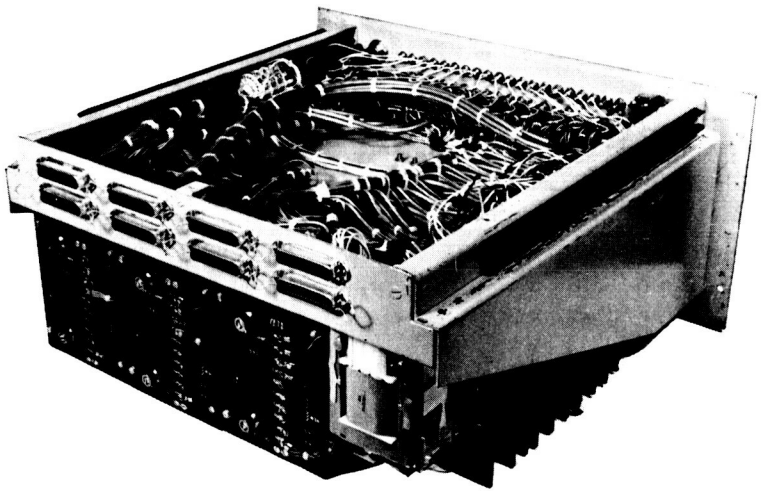


FIGURE 7-2 (CONT) MEMORY UNIT ELECTRONICS

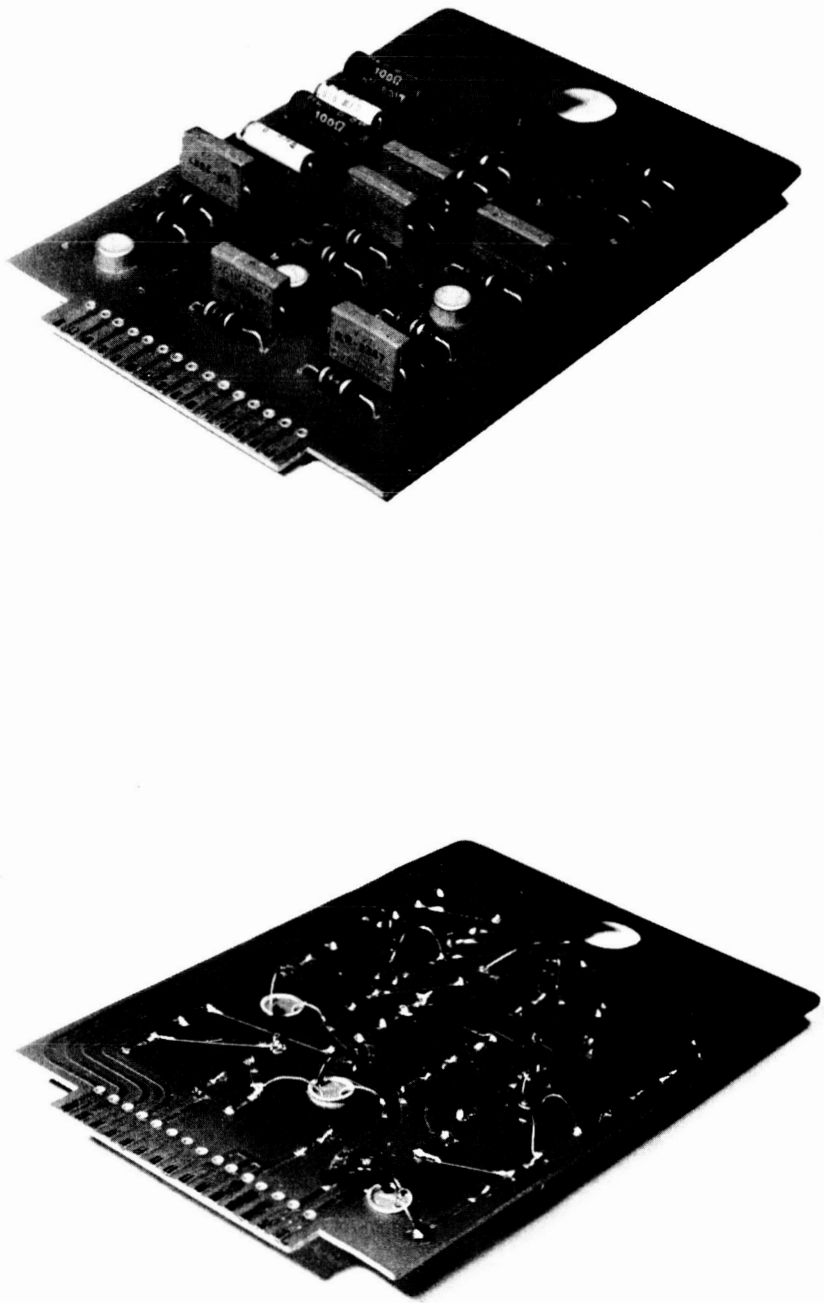


FIGURE 7-3 WRITE AMPLIFIER - MEMORY UNIT

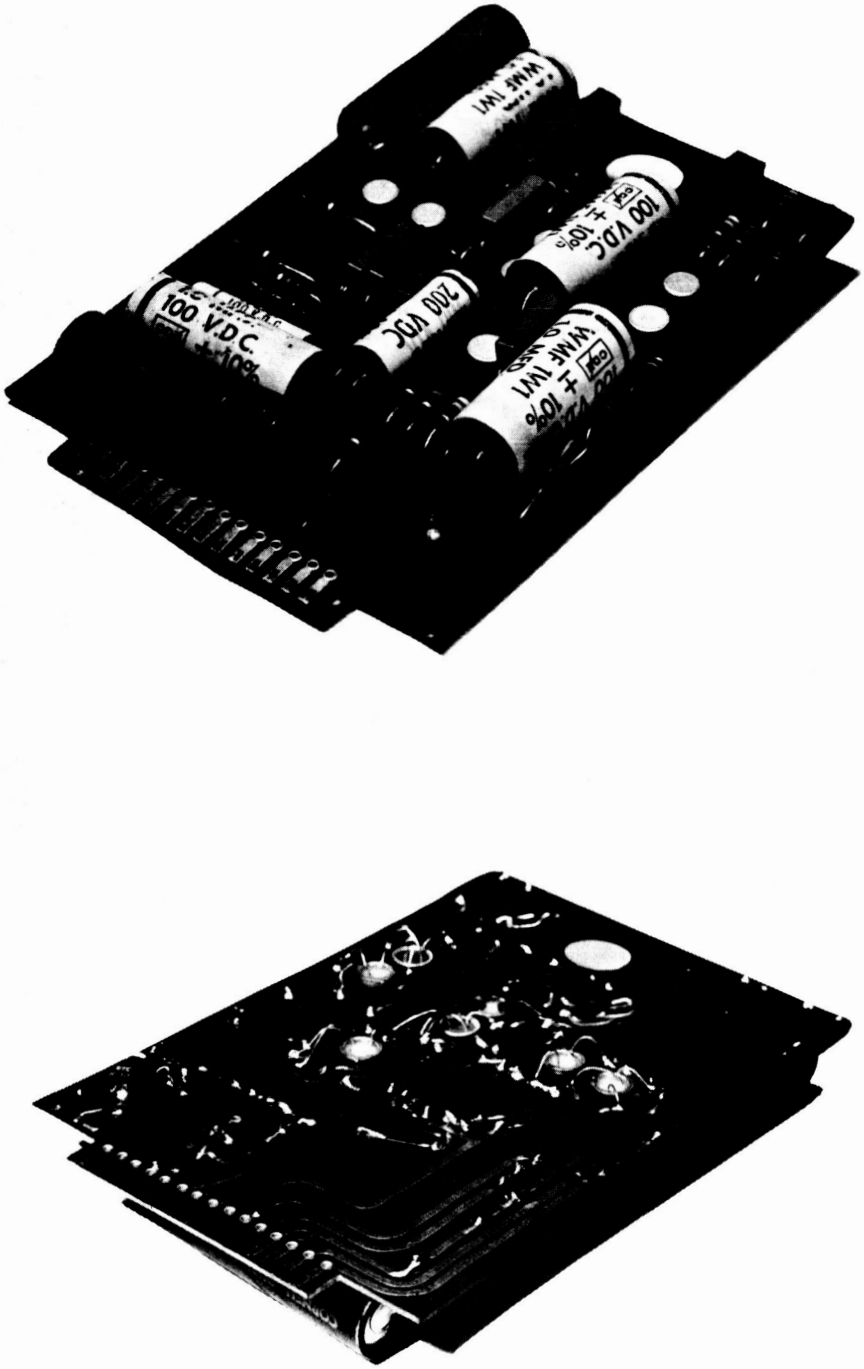
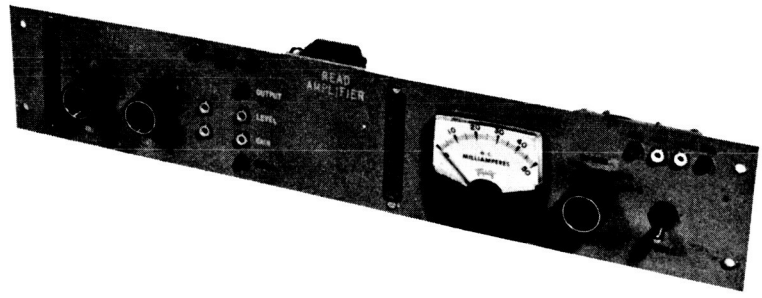


FIGURE 7-4 READ AMPLIFIER - MEMORY UNIT

FIGURE 7-5 MAGNETIC DRUM-MEMORY UNIT



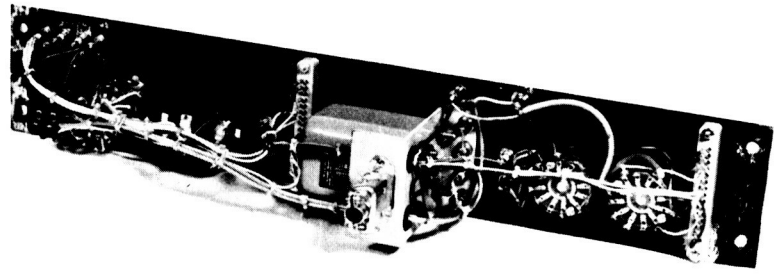


FIGURE 7-6 AMPLIFIER TEST UNIT

Control Unit

The control unit contains the clock logic, the address and word to be written circuitry, the display, the single drum-revolution control, reset, and program control auxiliary features described in Chapter VI. The control unit is shown in Fig (7-7). The bottom cover and internal wiring arrangement is similar to that shown for the memory unit.

The clock was experimentally verified as shown in Fig (7-8)(a) thru (n). The clock output pulses conforms to the timing requirements listed in Table 4-2.The amplitude scale is 10V/cm and the horizontal scale is given in each sub figure. In Fig (7-8)(a) the tach pulse can be seen. In addition, the period between basic time intervals is 12μsec. In Fig (7-8)(b) the pulses are the same except that the PROGRAM switch is now in the 2 position. Notice that the constant would now be read 12μ sec later, corresponding to a new address and different program. The time scale is compressed in Fig (7-8)(c) so that the complete time period of integrator O can be viewed. Notice that there are eight add pulses as required in Table 4-2.In Fig (7-8)(d), the time scale is further compressed so that a complete compensator cycle can be viewed. Notice that the pulse pattern is repetitious and that these pulses do not occur in the time periods for I8 and I9.

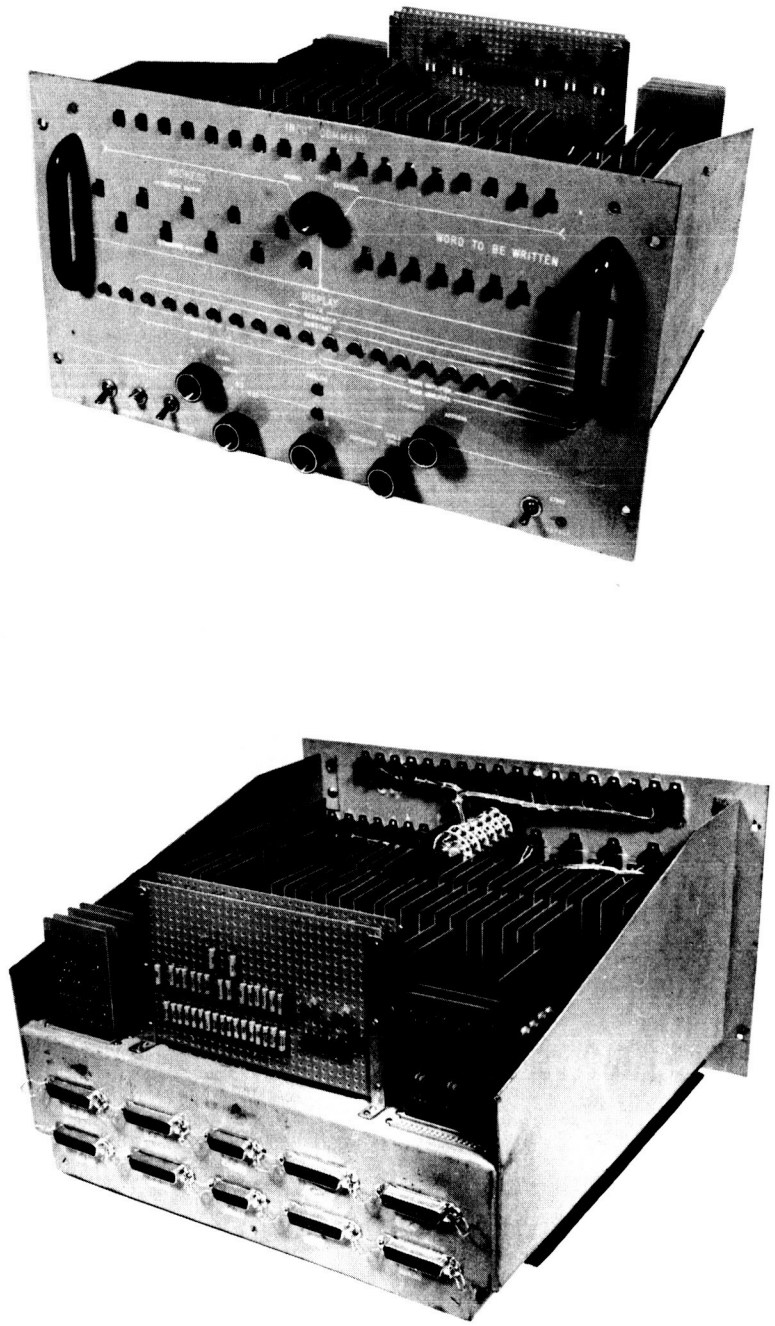
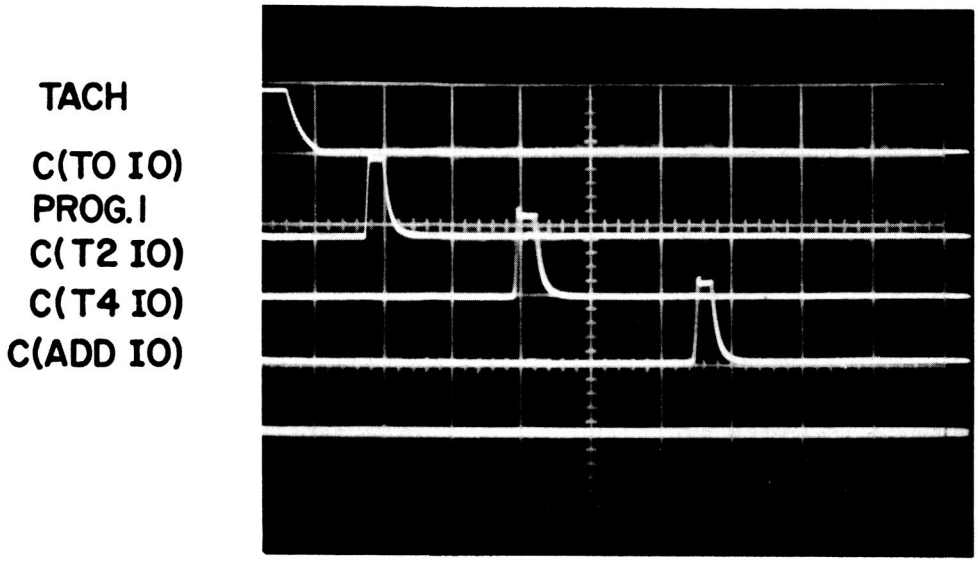
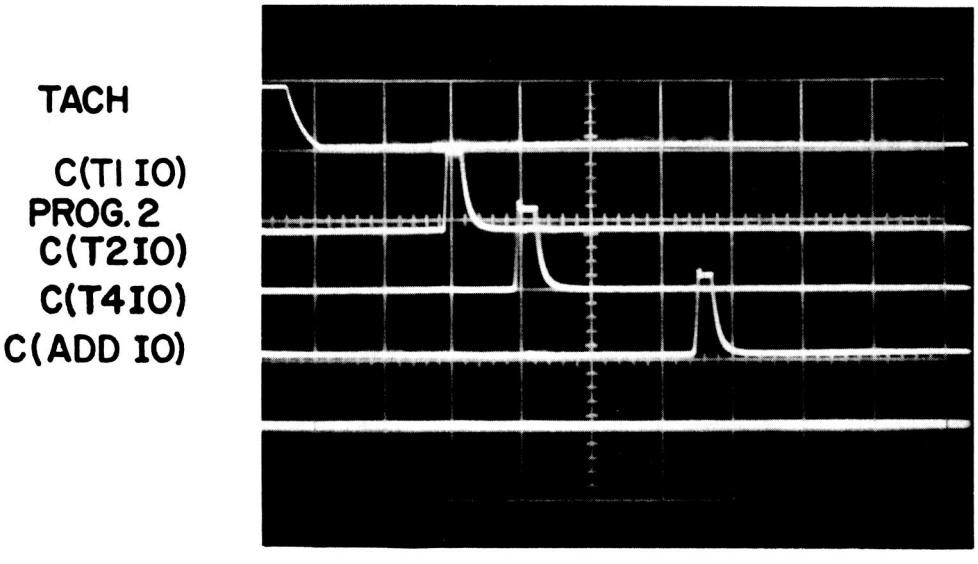


FIGURE 7-7 CONTROL UNIT



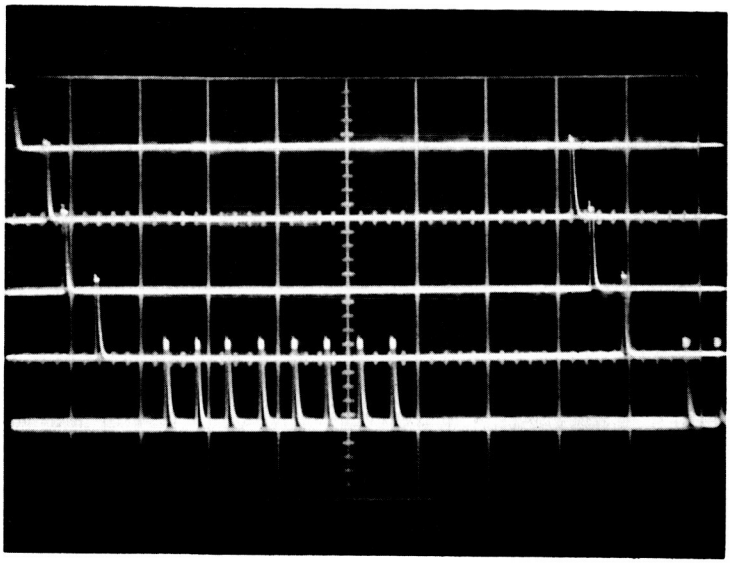
(a) 10μ SEC/CM



(b)

FIGURE 7-8 CLOCK PULSES

TACH
C(T1 IO)
C(T2 IO)
C(T4 IO)
C(ADD IO)



(c) 50μ SEC/CM

TACH
C(T1I-)
C(T2I-)
C(T4I-)
C(ADDIo)

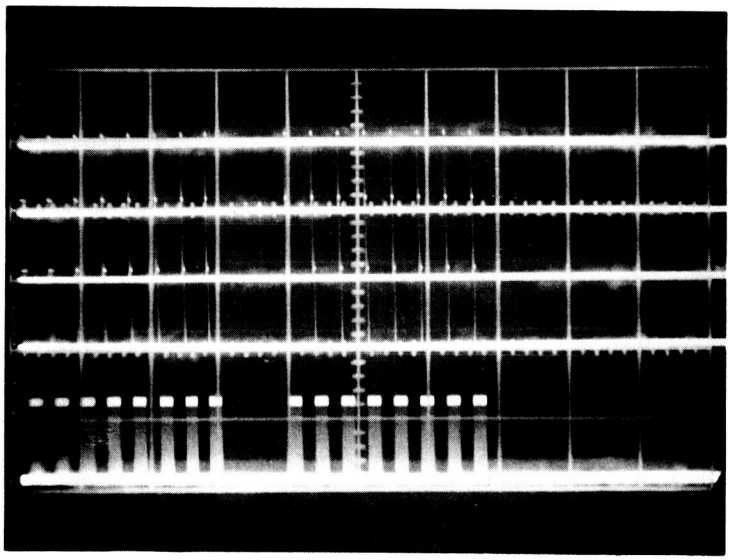


FIGURE 7-8 (con't) CLOCK PULSES

Fig (7-8)(e) shows the shift pulses spaced between the add pulses as required for multiplication. The write amplifier enable pulses can also be seen. In Fig (7-8)(f) the pattern repeats except for I8, I9, and I18. The enable pulses do occur during all integrator time periods.

Fig (7-8)(g) shows the last four pulses of integrator 1. Fig (7-8)(h) shows that these pulses do not occur in I8, I9 or I18.

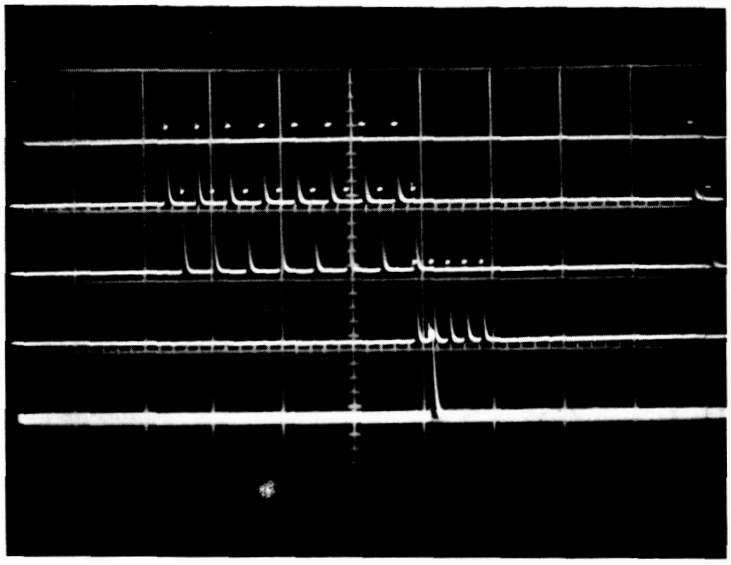
The timing pulses for I8 begin with Fig (7-8)(i). The top four traces are enlarged and correspond to the time where the lower trace is brighter. Notice that there are two timing pulses corresponding to C (TO I8). The second is delayed for 70 μ sec as required by the optical encoder logic. Fig (7-8) (k) shows that these pulses occur only during I8.

The pulses of I18 are shown in Fig (7-8)(m) and that these only occur during I18 can be seen in Fig (7 -8)(n).

The absence of pulse jitter can be seen from any of the figures since all patterns were operating continuously when the pictures were taken.

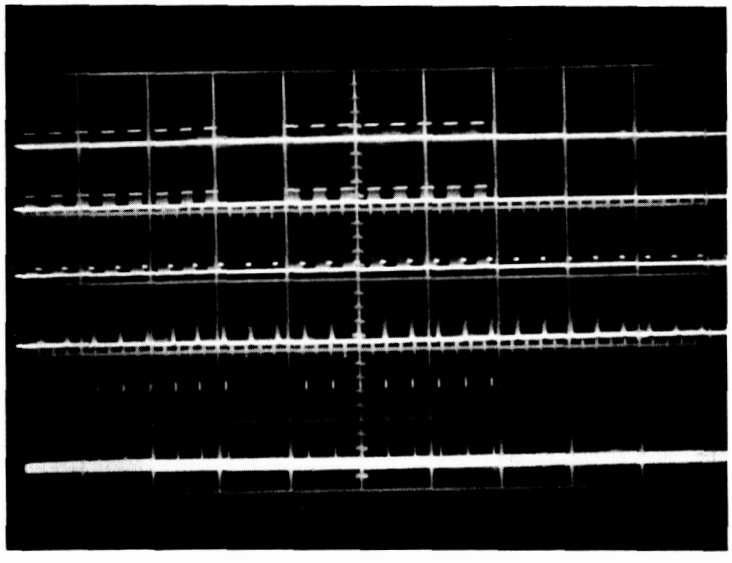
The other circuits of the control unit excluding display, were verified during the use of the memory unit.

TACH
C(ADD I1)
C(SHIFT I1)
ENABLE
C(T24I1)



(e) 50 μsec/cm

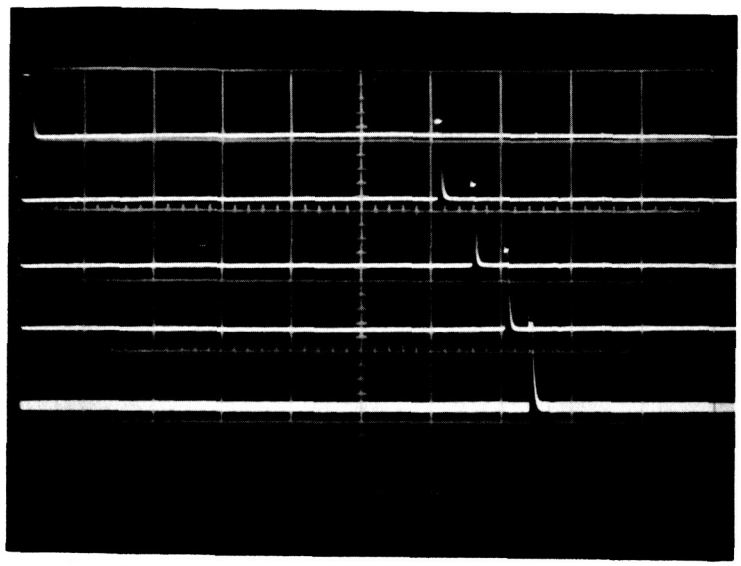
TACH
C(ADD I-)
C(SHIFT I-)
ENABLE
C(T24I-)



(f) 1ms/cm

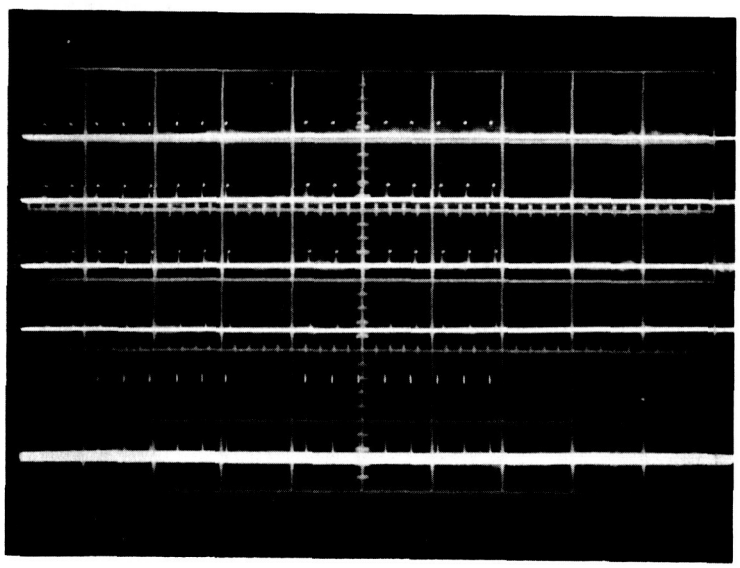
FIGURE 7-8 (CON'T) CLOCK PULSES

TACH
C(T24I-1)
C(T26I 1)
C(T28I1)
C(T30I1)



(g) 50 μsec/cm

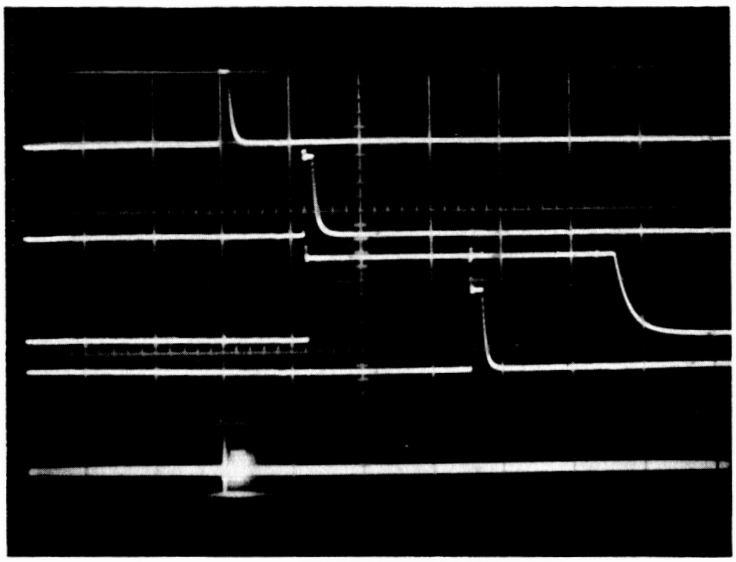
TACH
C(T 24I-)
C(T26I-)
C(T28I-)
C(T30I-)



(h) 1ms/cm

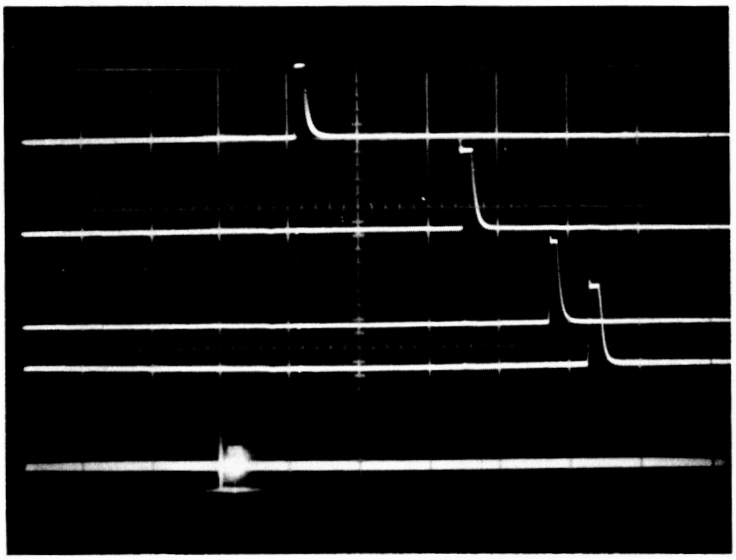
FIGURE 7-8 (CON'T) CLOCK PULSES

C(T3OI7)
C(TOI8)
C(TOI8) delayed
C(T4I8)
TACH (1ms/cm)



(i) 20 μsec/cm

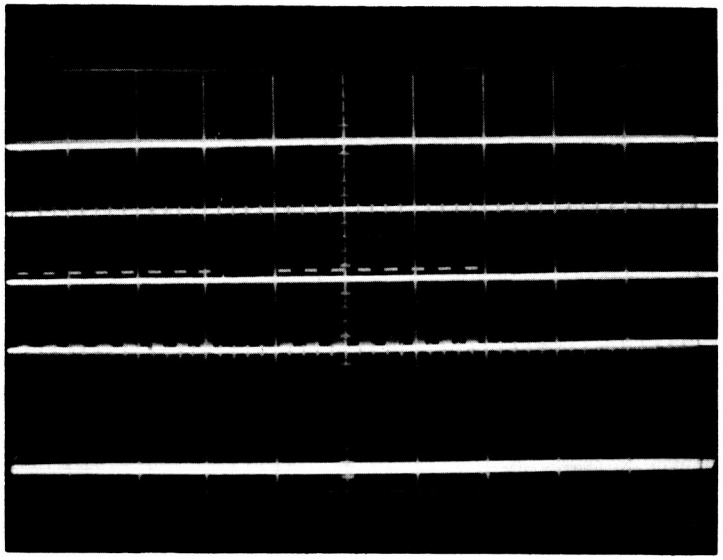
C(T3OI7)
C(T4I8)
C(T6I8)
C(T7I8)
TACH (1ms/cm)



(j) 20 μsec/cm

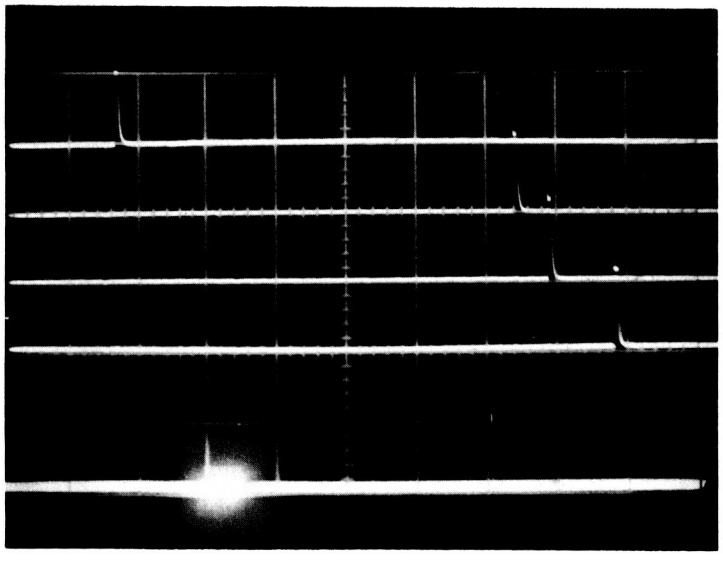
FIGURE 7-8 CON'T CLOCK PULSES

C(T 30I-)
C(T 4I8)
C(T 6I8)
C(T 7I8)
TACH



(k) 1ms/cm

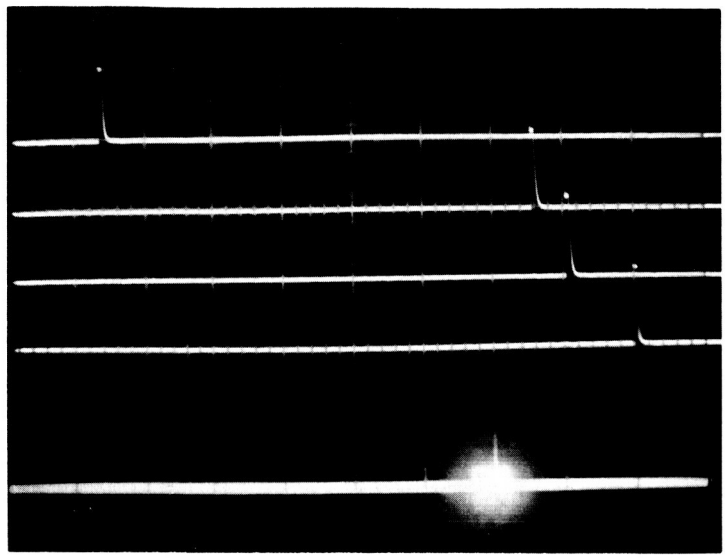
C(T 30I7)
C(T 24I8)
C(T 26I8)
C(T 30I8)



(l) 50 μsec/cm

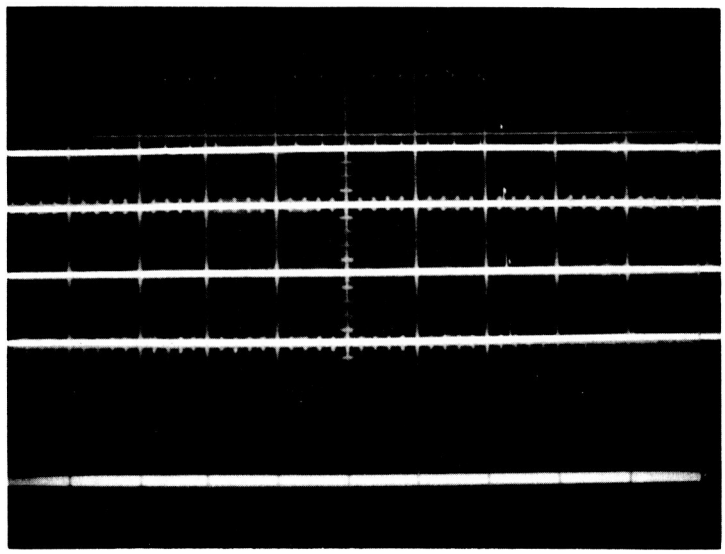
FIGURE 7-8 (CON'T) CLOCK PULSES

C(T30I17)
C(T24I18)
C(T26I18)
C(T30I18)
TACH (1ms/cm



(m) 50 μsec/cm

C(T30I-)
C(T24I18)
C(T26I18)
C(T30I18)
TACH



(n) 1ms/cm

FIGURE 7-8 (CON'T) CLOCK PULSES

Arithmetic Unit

The arithmetic circuits are contained in the arithmetic unit which can be viewed in Fig (7-9). The circuits were verified by repeatedly adding words of alternating ONES until all combinations were tested. The NOR-3 logic element used in conjunction with the full adder-subtractor and shown in Fig (5-7) is also located in the Arithmetic Unit.

Multiplication was verified by testing many sample problems. The multiplication time is limited by the add and shift clock periods.

Digital to A-C Converter

The digital to a-c converter occupies the two boards mounted on the servo electronics panel shown in Fig (7-10). A linearity test was conducted. The results are given in Table 7-1. Examination of the results indicates that the output is linear, within experimental accuracy, except for a 70 mv offset on one side. This offset is attributed to both sides of the center tapped transformer not having the same number of turns. The transformer used was a filament power supply transformer. The two lowest digits are not connected in the system so the offset represents 2 units from a full scale of 256 units.

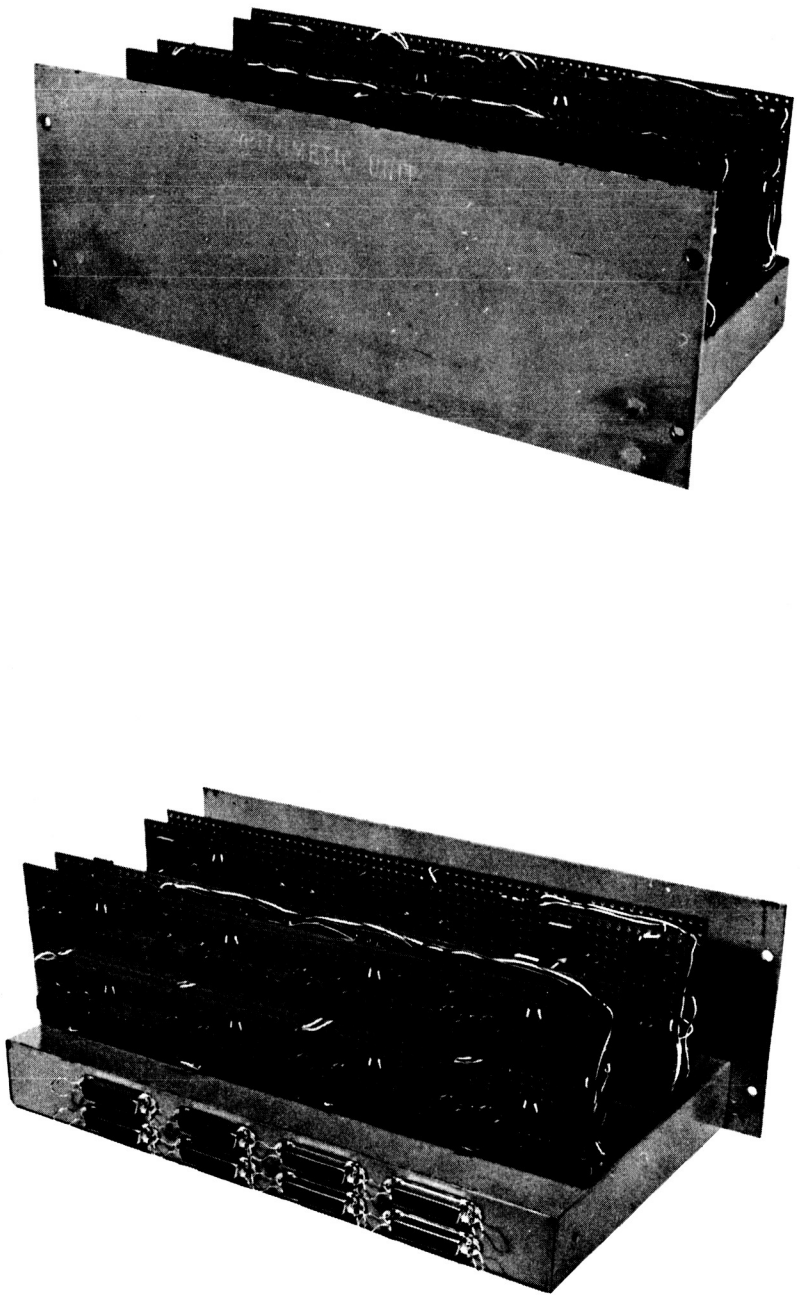
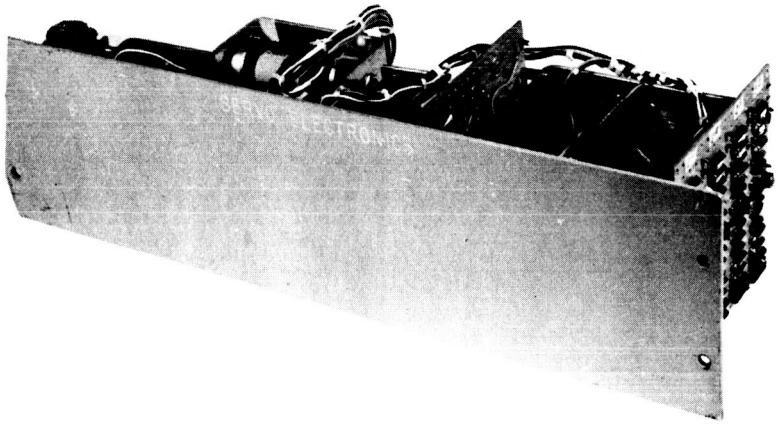


FIGURE 7-9 ARITHMETIC UNIT



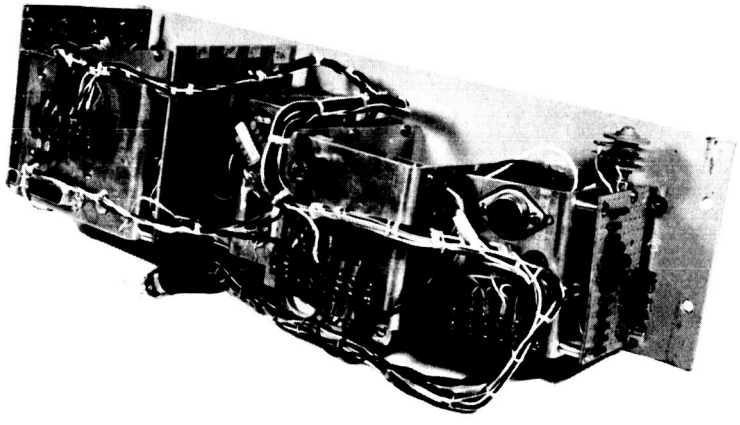


FIGURE 7-10 SERVO ELELECTRONICS UNIT

Table 7-1
Digital to A-C converter
Test Results

Switch Positions											Digital	Converter
SIGN	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Number	Output, mv
0	1	0	0	0	0	0	0	0	0	0	+ 512	3,840
0	0	1	0	0	0	0	0	0	0	0	+ 256	1,920
0	0	0	1	0	0	0	0	0	0	0	+ 128	960
0	0	0	0	1	0	0	0	0	0	0	+ 64	480
0	0	0	0	0	1	0	0	0	0	0	+ 32	240
0	0	0	0	0	0	1	0	0	0	0	+ 16	120
0	0	0	0	0	0	0	1	0	0	0	+ 8	60
0	0	0	0	0	0	0	0	1	0	0	+ 4	30
0	0	0	0	0	0	0	0	0	1	0	+ 2	15
0	0	0	0	0	0	0	0	0	0	1	+ 1	7
												OFFSET
1	0	0	0	0	0	0	0	0	0	1	- 1	7 + 70
1	0	0	0	0	0	0	0	0	1	0	- 2	15 + 70
1	0	0	0	0	0	0	0	1	0	0	- 4	30 + 70
1	0	0	0	0	0	0	1	0	0	0	- 8	60 + 70
1	0	0	0	0	0	1	0	0	0	0	- 16	120 + 70
1	0	0	0	0	1	0	0	0	0	0	- 32	240 + 70
1	0	0	0	1	0	0	0	0	0	0	- 64	480 + 70
1	0	0	1	0	0	0	0	0	0	0	- 128	960 + 70
1	0	1	0	0	0	0	0	0	0	0	- 256	1,920 + 70
1	1	0	0	0	0	0	0	0	0	0	- 512	3,840 + 70

Servoamplifier

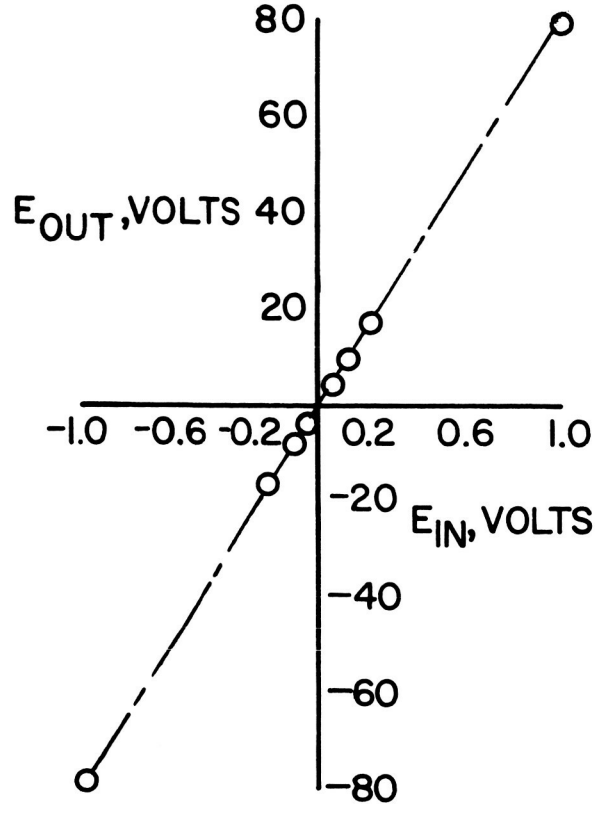
The performance of the servoamplifier is characterized by its frequency response, the linearity of its output and the fidelity of its waveforms.

The experimental open and closed loop frequency response curves are shown in Fig (5-12). The closed loop response is nominally 10 cps to 900 cps. An amplitude modulated carrier leads to two sidebands which are symmetrical with respect to the carrier frequency. A flat response on both sides of 60 cps is required. The amplitude modulated band width is nominally 50 cps. The tests were conducted using the servomotor as a load.

The linearity of the servoamplifier is given in Fig (7-11)(a). The input and output voltages were measured peak-to-peak. The fidelity of the servoamplifier can be seen in Figs (7-11)(b), (c) and (d). During high performance operation the sidebands do not exceed 30 cps from the carrier frequency.

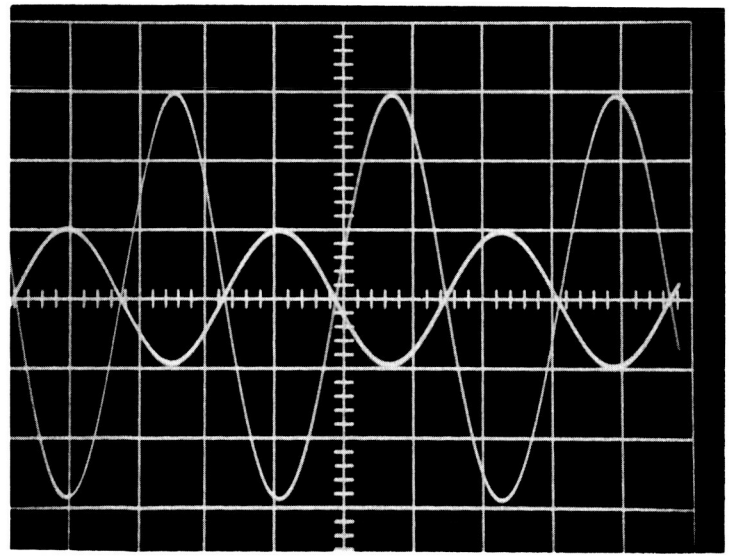
Encoder Electronics

The electronics for the encoders is shown in Fig (7-12). The encoder electronics are commercial except for the necessary power supplies and the encoder coupling discussed in Chapter VI.



(A) LINEARITY OF SERVOAMPLIFIER

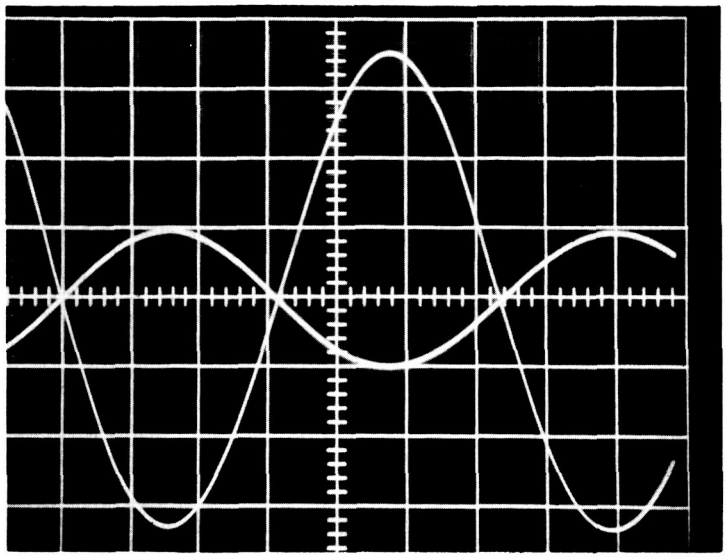
TIME BASE 5ms/cm
VERTICAL
INPUT 0.2v/cm
OUTPUT 10.5v/cm



(B) 60 CPS WAVEFORM

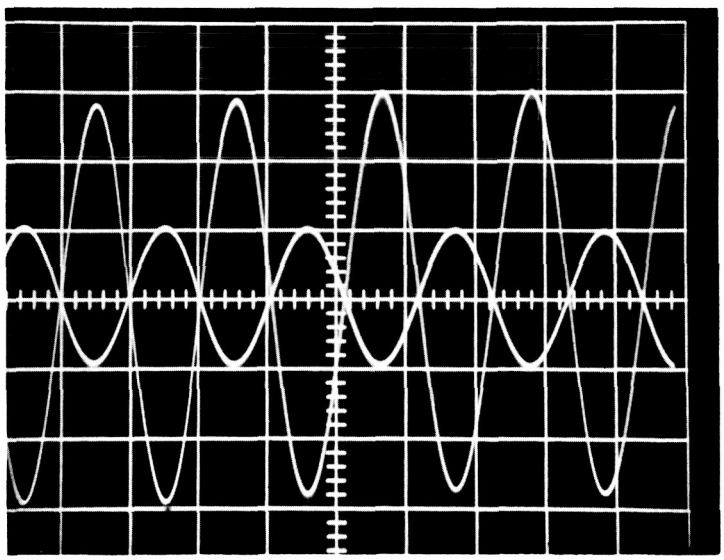
FIGURE 7-11 SERVOAMPLIFIER LINEARITY AND FIDELITY

TIME BASE 5ms/cm
VERTICAL
INPUT 0.2v/cm
OUTPUT 10.5v/cm



(c) 30 cps

TIME BASE 5ms/cm
VERTICAL
INPUT 0.2v/cm
OUTPUT 10.5v/cm



(d) 90 cps

FIGURE 7-11 (CONT'D) SERVOAMPLIFIER LINEARITY & FIDELITY

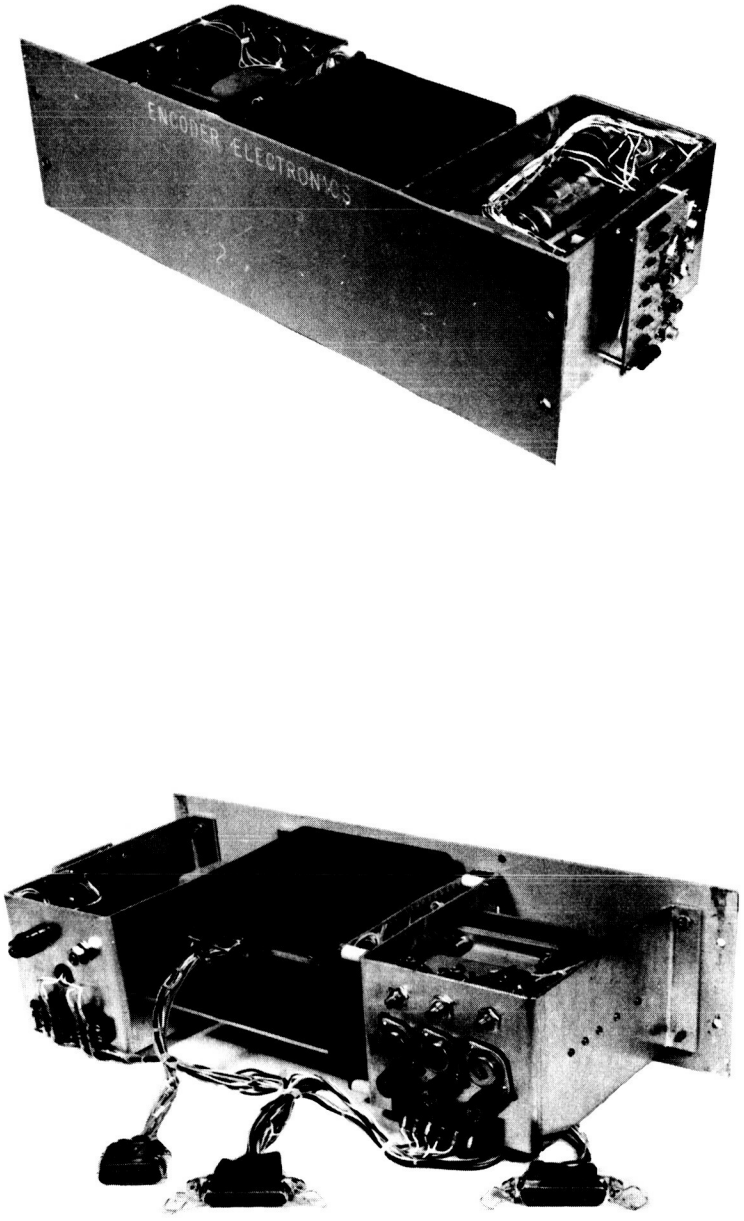


FIGURE 7-12 ENCODER ELECTRONICS UNIT

Plant Simulator

The plant simulator is shown in Fig. (7-13). The plant is minimal in that it consists of a motor, gear train and absolute data encoders. There is no external load so that the dynamic response is as large as possible. This situation is usual in instrument servomechanisms where the controlled variable is a shaft position. In order to obtain a visual resolution commensurate with the encoder resolution, (1 part in 65, 536), the shaft position is displayed on two dials. The fine dial includes a vernier which indicates the shaft position to a resolution of 12 minutes. The coarse dial is divided into 50 segments where each segment corresponds to one turn of the fine dial. The shaft position indicated by the fine and coarse dials, can be viewed through the windows of the cover.

The gears are mounted between the bearing plates shown in Fig. 7-13. The bearing plates are made of aluminum so that under high temperature operation the gear train does not tend to bind due to the thermal exponsion of the aluminum bearing plates. Notice, that when the cover is in place, the gear train is totally enclosed.

To obtain the dynamic characteristics of the plant and servoamplifier combined, the open loop frequency response was determined using a modulated 60 cps carrier driving signal from a Servoscope. The shaft motion was measured by means

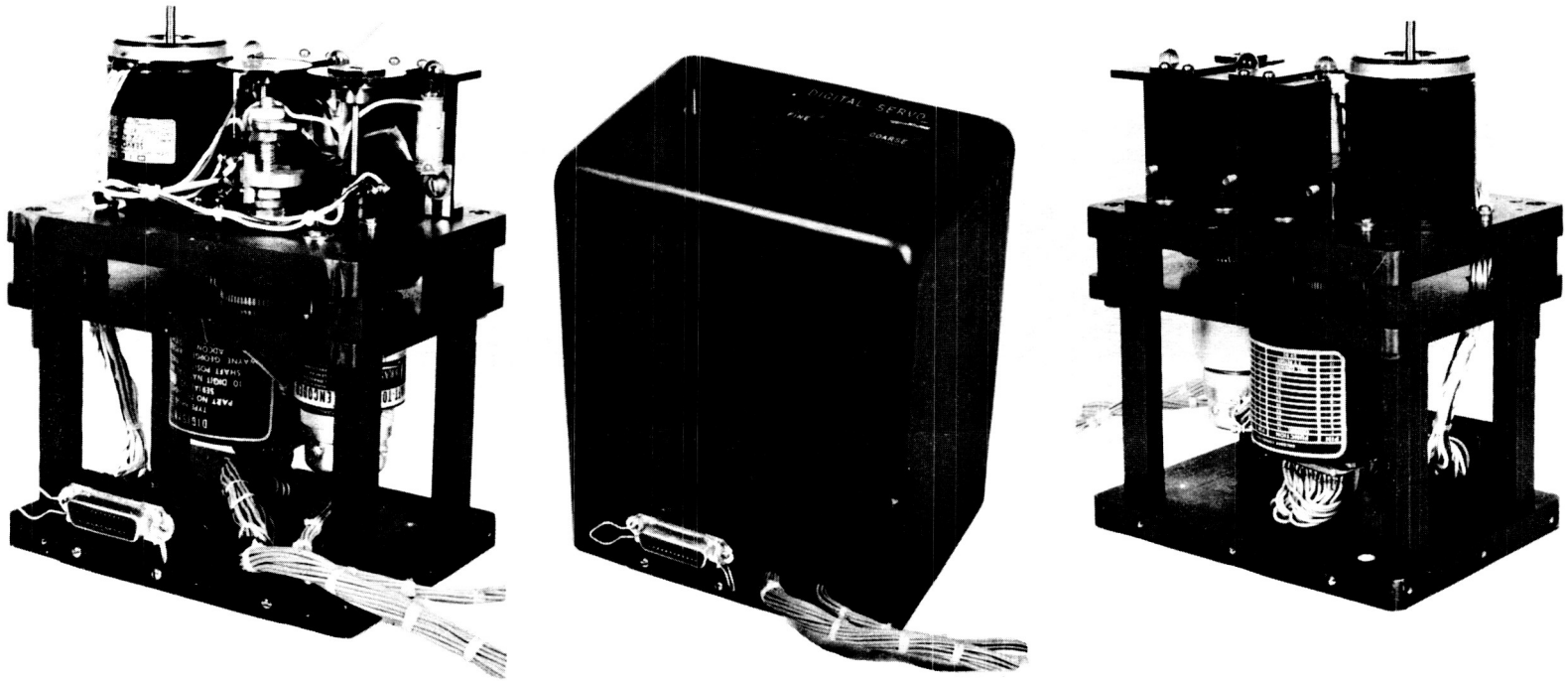


FIGURE 7-13 PLANT SIMULATOR

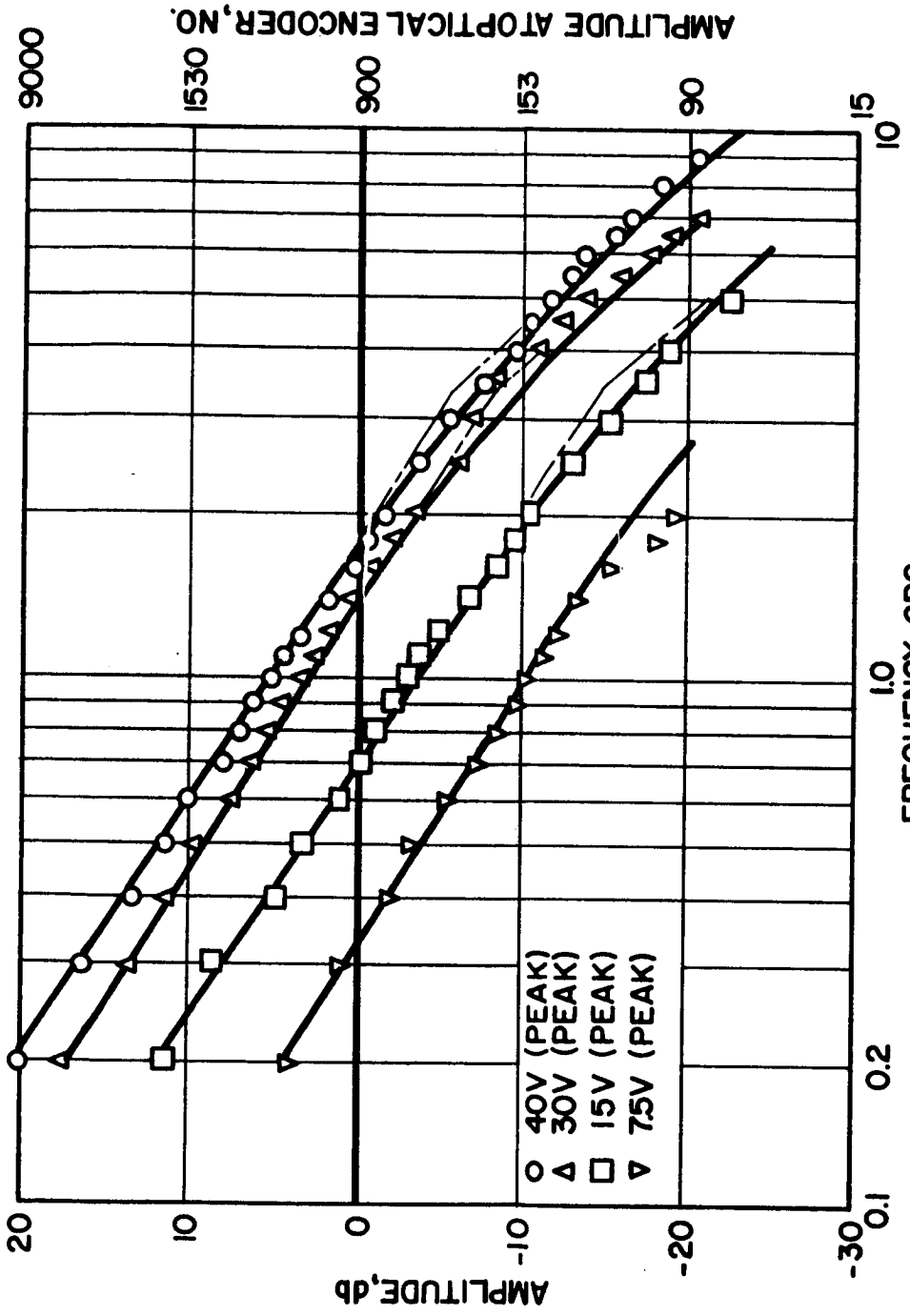


FIGURE 7-14 PLANT FREQUENCY RESPONSE

of the analog potentiometers mounted on the dial shafts visible in Fig. (7-13).

The results are shown in Fig. (7-14). The 20 db/ decade low frequency slope is characteristic of an integrator as provided by the servomotor. Experimental data was obtained at 100 per cent, 75 per cent, 38 per cent, and 19 per cent of full excitation. Full excitation corresponds to a 40 volt peak voltage limited by the power supply. The dashed-dot lines shown correspond to a straight line attentuation diagram. The correct curve is drawn 3db down at the break point of the straight line diagram. It can be seen that with full excitation there is a well defined break point at 3. 4 cps corresponding to the torque to inertia ratio. At 75 per cent and 38 per cent of full excitation the breakpoint is still well defined. At 19 per cent excitation the response droops sooner probably due to the increased importance of Coulomb friction. However, this is also at the limit of accurate experimental measurements.

The 3. 4 cps break point was used in calculating the transfer function of the plant as given in Appendix A.

In a general testing program it is desirable to be able to change the plant break point. This can be done easily by mounting an inertia wheel on the motor shaft which protrudes through the cover. Any inertia which is added at a point further out in the gear train is less effective in changing the break point since it is reduced by the gear ratio squared.

The second time constant is provided by the servo-amplifier. The bandwidth can be changed by reducing both the low frequency and high frequency break points. It is suggested that the 48μfd capacitor which tunes the motor be decreased to reduce the low frequency response and a capacitor be placed between the base of the driver transistor and ground to reduce the high frequency response.

By adding an inertia wheel and changing capacitors in the servoamplifier, a variety of plant characteristics can be studied.

VIII. RECOMMENDATIONS FOR FURTHER WORK

An extensive testing program should be conducted to thoroughly evaluate the performance of the compensator. In addition to ramp and step inputs the plant can be programmed to obtain a constant velocity output. This can be accomplished with a similar analysis and requires only a changing of the constant coefficients recorded on the drum.

The effect of longer sample periods could be experimentally verified by the use of the SAMPLE PERIOD feature in the control unit. The coefficients on the drum would again be changed based upon an analysis where T would be replaced by 2T and 4T.

The frequency response of the compensated plant could be obtained with the use of the EXTERNAL input command switch and a sinusoidally driven encoder.

The clock pulses are 3 μ sec wide but the basic period in the present design is 12 μ sec. By by-passing the first FF in the clock counter, the system computation time could be reduced by a factor of 2. This would allow the compensator to compensate 10 plants simultaneously.

Experiments pertaining to a supervisory computer

switching programs and writing new programs while it is compensating a plant could also be done.

APPENDIX A

It has been shown, eqn(1-15), that the sampled response for sampled and held inputs can be obtained from

$$G^*(Z) = (1-Z^{-1}) \quad Z \left\{ \frac{G(p')}{p} \right\} \tag{2-15}$$

G(p) has been shown to have the following form, eqn. (2-19).

$$G(p) = \frac{K}{p(1 + T_A p)(1 + T_L p)} \tag{2-19}$$

$$\therefore \frac{G(p)}{p} = \frac{K}{p^2(1 + T_A p)(1 + T_L p)}$$

The Z-transform of this expression can be obtained by a partial fraction expansion of the equation and then using a simple table to Z-transform each term[12].

$$\frac{G(p)}{p} = \frac{C_{11}}{p^2} + \frac{C_{12}}{p} + \frac{C_2}{1 + T_A p} + \frac{C_3}{1 + T_L p} \tag{A-1}$$

$$C_{11} = \left. \frac{K}{(1 + T_A p)(1 + T_L p)} \right|_{p = 0} = K \tag{A-2}$$

$$C_{12} = \frac{d}{dp} \left[\frac{K}{(1 + T_A p)(1 + T_L p)} \right]_{p=0}$$

$$= - K \left. \frac{\left[(1 + T_A p)\, T_L + (1 + T_L p)\, T_A \right]}{\left[(1 + T_A p)(1 + T_L p) \right]^2} \right|_{p=0}$$

$$C_{12} = - K \left[T_L + T_A \right] \tag{A-3}$$

$$C_2 = \left.\frac{K}{p^2(1 + T_L p)}\right|_{p = -\frac{1}{T_A}} \qquad (A\text{-}4)$$

$$C_2 = \frac{KT_A^2}{\left(\frac{1 - T_L}{T_A}\right)}$$

$$C_3 = \left.\frac{K}{p^2(1 + T_A p)}\right|_{p = -\frac{1}{T_L}} \qquad (A\text{-}5)$$

$$C_3 = \frac{KT_L^2}{\left(\frac{1 - T_A}{T_L}\right)}$$

$$\therefore \frac{G(p)}{p} = K\left[\frac{1}{p^2} - \frac{(T_L + T_A)}{p} + \frac{T_A^2}{\left(\frac{1-T_L}{T_A}\right)\left(1 + T_A p\right)} + \frac{T_L^2}{\left(\frac{1-T_A}{T_L}\right)\left(1+T_L p\right)}\right]$$

substituting $T_A = 0.003$

$T_L = 0.045$

$$\frac{G(p)}{p} = K\left[\frac{1}{p^2} - \frac{(.048)}{p} - \frac{0.64.10^{-6}}{(1 + 0.003p)} + \frac{2025.13.10^{-6}}{(1 + .045p)}\right] \qquad (A\text{-}6)$$

$$\frac{G(p)}{p} = K\left[\frac{1}{p^2} - \frac{0.048}{p} - \frac{0.21 \cdot 10^{-3}}{333 + p} + \frac{44.96 \cdot 10^{-3}}{22.2 + p}\right] \qquad (A\text{-}7)$$

but [3]

$$Z\left[\frac{1}{p^2}\right] = \frac{TZ^{-1}}{(1-Z^{-1})^2} \qquad (A\text{-}8)$$

$$Z\left[\frac{1}{p}\right] = \frac{1}{(1-Z^{-1})} \qquad (A\text{-}9)$$

$$Z\left[\frac{1}{a+p}\right] = \left[\frac{1}{(1-3^{aT}Z^{-1})}\right] \qquad \text{(A-10)}$$

$$Z\left[\frac{G(p)}{p}\right] = K\left[\frac{TZ^{-1}}{(1-Z^{-1})^2} - \frac{0.048}{(1-Z^{-1})} - \frac{0.21\cdot 10^{-3}}{(1-e^{-333T}Z^{-1})} + \frac{44.96\cdot 10^{-3}}{(1-e^{-22.2T}Z^{-1})}\right] \qquad \text{(A-11)}$$

In this system the sampling period T is taken to be the time required for one revolution of the drum. Since the motor is nominally 3600 rpm with a 7 per cent slip, T was measured to be 0,018 sec.

$$\therefore Z\left[\frac{G(p)}{p}\right] = K\left[\frac{0.018Z^{-1}}{(1-Z^{-1})^2} \quad \frac{-0.048}{(1-Z^{-1})} \quad \frac{-0.21\cdot 10^{-3}}{(1-0.0025Z^{-1})} + \frac{44.96\cdot 10^{-3}}{(1-0.67Z^{-1})}\right] \qquad \text{(A-12)}$$

(A-12)

by expanding, grouping and factoring,

$$(1-Z^{-1})\,Z\left[\frac{G(p)}{p}\right] = \frac{0.002290\,KZ^{-1}(1+1.4811\,Z^{-1})(1+0.0451\,Z^{-1})}{(1-Z^{-1})(1-0.67Z^{-1})(1-0.0025Z^{-1})} \qquad \text{(A-13)}$$

APPENDIX B

Logic of the V-Brush Method

A logical method for reading out unambiguously a natural, binary-coded disk came about from observations of the particular nature of the binary code.[17]

Examination of Table B-1 shows that, when the least significant digit (LSD) changes from 0 to 1 in the increasing count direction, none of the other digits change. Furthermore, when LSD changes from 1 to 0, the digit in the next most significant column always changes. In general then, when the digit in the n^{th} row changes from 1 to 0, the $(n^{th} + 1)$ digit always changes.

Fig B-1 shows that, when LSD is 1, the next column has not changed its count for a minimum of the width of an LSD. Further observation of the code

				← LSD Column
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
		etc.		

Table B-1 Binary Number System

pattern leads to the generalization that, when a digit in the n^{th}

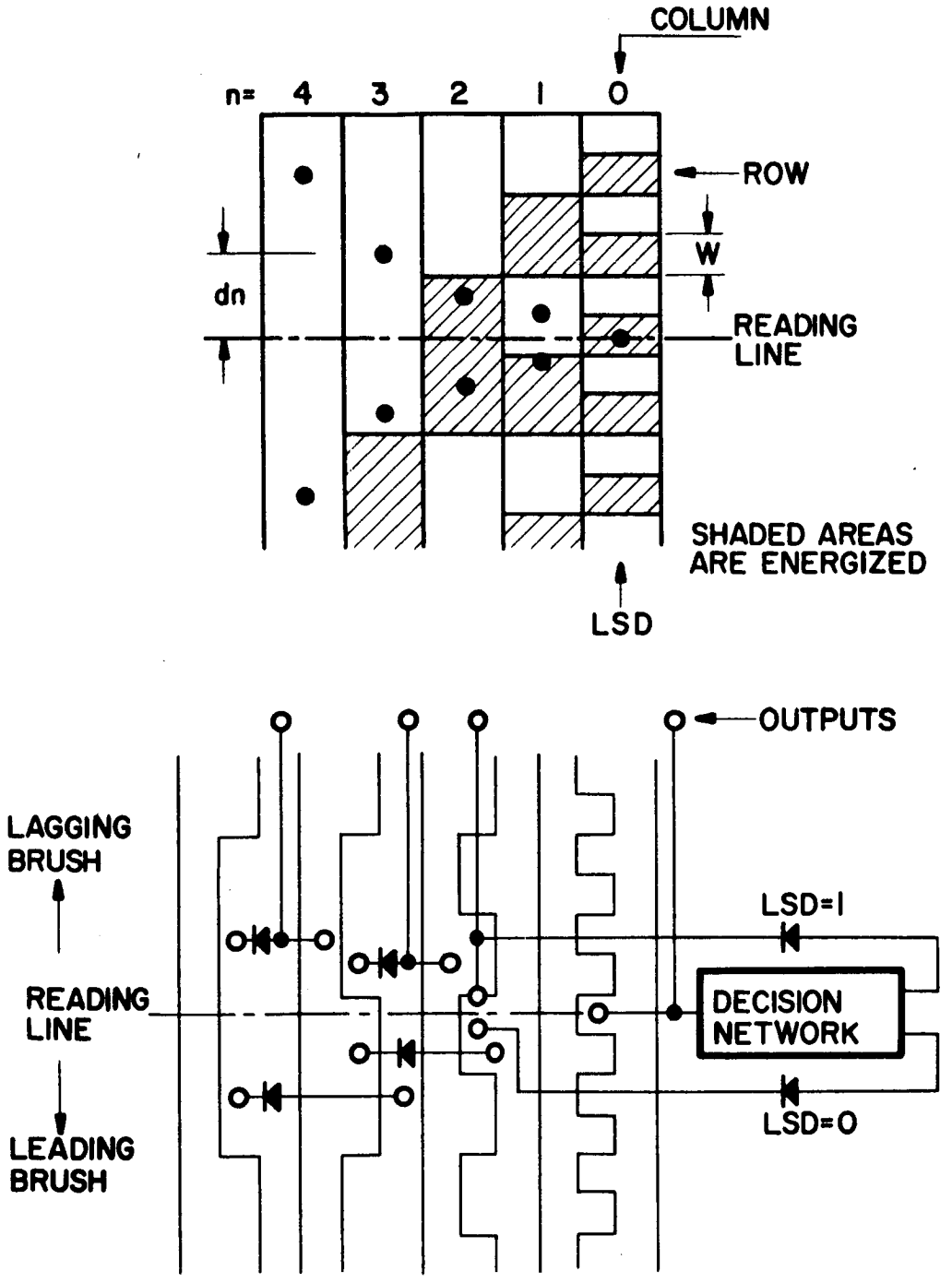


FIGURE B-1 SELF SELECTION SCHEME FOR "V-SCAN"

column is a 1, the digit in the (n+1) column has not changed for a minimum of 2^n rows.

Based upon these conclusions, a method evolves for reading a natural binary-code pattern unambiguously, which is based upon this reasoning: if a ONE is read in the LSD, then, in the increasing count direction, no change in the next digit to the LSD has occured recently. If the ZERO is read in the LSD then a change has occurred recently in the next to LSD (NLSD). Therefore, if there were two brushes to read the (NLSD), one lagging and one leading the reading line, it would be a simple matter to read either the recent "change" or "no change" condition. From the foregoing, we would read the leading brush if LSD=0, and the lagging brush if LSD=1. So this scheme provides a way in which the reading of the (NLSD) can be anticipated based upon the reading of the LSD, with all switching done by the LSD.

If we were to remove the LSD column (Fig B-1) the remaining pattern is still natural binary but the LSD unit is larger. Therefore, the reasoning we have just used for the NLSD applies also to the next to the NLSD (NNLSD), based upon the reading of the NLSD. Hence, if NLSD=1, the lagging brush of NNLSD is read: if NLSD=0, then the leading NNLSD is read. And so on to the most significant digit.

It has been found that the brushes should be symmetrically located about the reading line, with the brush-to-brush spacing for a given digit equal to the segment width of the NLSD. The brushes then fan out from the reading line on a V-shaped exponential

curve, where the distance d_n from the reading line is given by the relation

$$d_n = \pm \frac{1}{2} (2^{n-1} W) \qquad \text{(B-1)}$$

where W is the segment width of the LSD.

The number to be read on the reading line is 00101. Since the LSD=1 (column 0), we read the lagging brush in column 1. This brush reads 0, so we read the leading brush in column 2. This reading is a 1, so we read the lagging brush in column 3, which reads a zero, so we read the leading brush in column 4. Hence the number read out is 00101. Note that every reading brush is well within the segment which it is reading.

The only difficulty with the method outlined is that, for each column to be read, a logical circuit is required to decide, based upon the preceding reading, whether the leading or lagging brush should be read. The next logical step is to arrange and interconnect the brushes such that they themselves will automatically select the proper leading or lagging brush. To do this, each digit column is separated into two zones, called ZERO and ONE zones as shown in Fig B-1.

The brushes are then wired so that the brush riding permanently in the ONE zone of the n^{th} digit is connected to the lagging commutator brush in the n+1 digit, as shown in Fig B-1. With this arrangement, the rule for reading out a natural binary pattern with V-brushes is automatically obeyed. The rule: "If the n^{th} digit is a ONE, read the n+1 lagging brush; if the n^{th} digit is a ZERO, read the n+1 leading brush."

For the wiper position shown, the LSD (column 0) is a ZERO, and hence, column 1 leading brush is selected. Column 1 output is 0, so column 2 leading brush is selected. Column 2 output is 1 so column 3 lagging brush is selected. Column 2 output is 1 so column 3 lagging brush is selected. The natural binary output is then 0100.

Since this self-selecting method is identical in logic with the ordinary V-brush method, the output is always nonambiguous. All changes in output are initiated through the LSD.

Note that the input brush on the reading line must make contact with either a ONE zone or a ZERO zone. This would require that there be no insulation between the zones. If this were true, the zones would no longer be electrically divided. Therefore, it is necessary to use an external decision circuit. The leading or lagging brush for column 1 is selected externally. In this application column 0 is by-passed and column 1 is selected by column 9 of the optical encoder.

APPENDIX C

MEMORY UNIT

Introduction

Magnetic recording on rotating drums is an economical, efficient and widely accepted technique for storing information in a high-speed data handling device. The basic principle is that a small area of the magnetic coating on a drum is magnetized in either one of two senses representing, for logical purposes, the binary information ZERO and ONE. The magnetic characteristics of the storage medium are such that stored information is non-volatile, i.e., does not change in any way without subsequent external cause.

Small electromagnets, rigidly mounted near the surface of the drum, serve as transducers between the magnetic storage system and the rest of the electrical data handling system. These electromagnets, called heads, serve both to write information on the drum and to read stored information from it. Each head is associated with one circumferential track on the drum. More than one head, as in the present application, may be mounted on the same track.

The core and winding of a typical head is shown in Fig C-1.

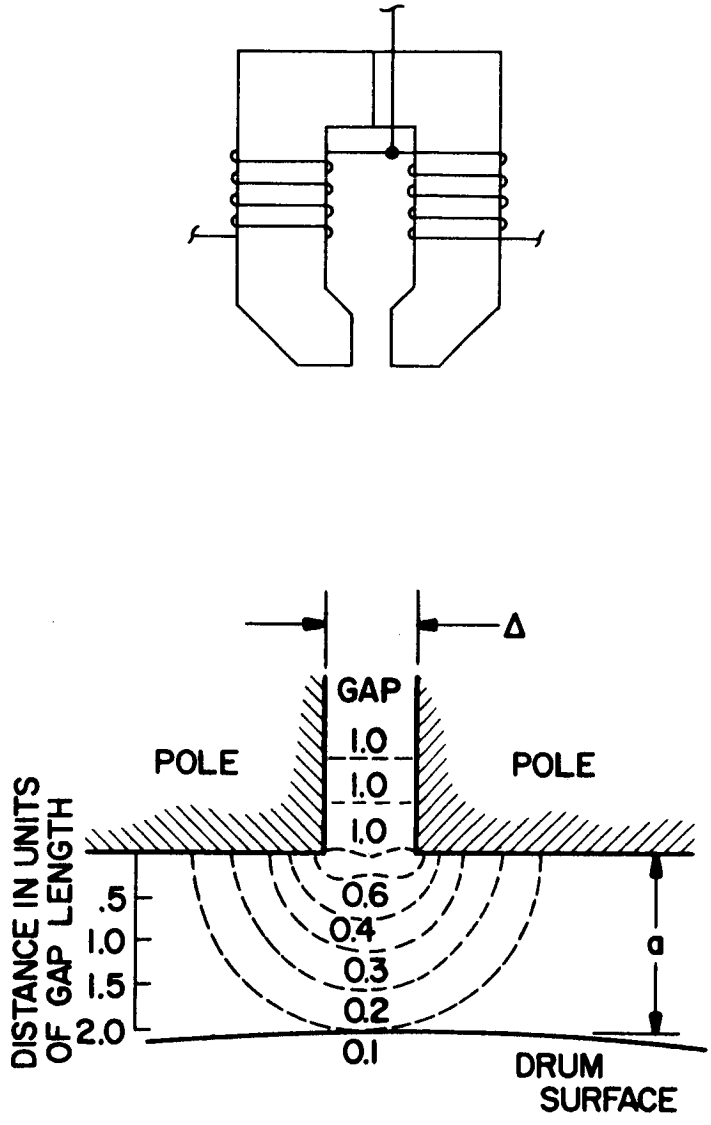


FIGURE C-1 MAGNETIC HEAD & FLUX DISTRIBUTION

In the process of writing binary information on the surface of a drum,, a current pulse through one side of the coil magnetizes the core of the head in one of the two polarity directions. The purpose of the gap in the front of the head is to help generate a strongly localized field that acts only over a small region of the medium. As the magnetizing current is increased there is a tendency for the head tips to saturate as shown in Fig C-1. This makes the effective air gap larger than its geometrical size. The irregularities of the gap surfaces themselves provide enough spacing for successful writing. However, decreasing δ, also decreases the maximum "a" required for successful operation.

The field deep in the gap is of strength 100%. The field decreases with distance from the gap. Notice that the field for a given strength also becomes wider in front of the gap.

In the process of reading the head acts as a generator. As a magnetized area of information approaches and recedes from the head by virtue of the drum rotation, flux increases and decays in the head core, inducing corresponding voltage transients at the terminals of the coil used for reading. The voltage induced in the head windings has characteristics dependent on whether the area then under the head contains a ONE or a ZERO.

If a coated surface is placed in front of the gap at a distance

from the head equal to one gap length, "a" equals δ, then the maximum field that the edge of the coating nearest the head can encounter is about 28% of that present deep in the head gap. See Fig C-1. Thus, to assure saturating the drum recording medium, the write current must produce sufficient flux in the gap that 28% of it will still saturate the drum. Notice that the area surrounding the saturation region is also affected. In fact the surface subjected to 10% of the gap flux is four times as wide as the gap. The factor of four applies to a stationary drum. In the present application the drum speed increases this factor to 14 if we use a 5 μ sec write pulse. This spreading effect is discussed later and gives rise to a "crowding" effect. Crowding occurs because a portion of a written pulse would be subjected to the field effects of the next pulse being written. It becomes less sharply defined and reduced in magnitude.

By designing the external electrical circuits so that the voltage at the terminals of the magnetic head is sampled only when the desired area is producing that voltage, it becomes possible to read the contents of any desired area. Reading may be repeated an infinite number or times without causing any deterioration of the magnetization.

Providing the magnetizing force exceeds the coercive force of the recording medium, when a ONE is written over a previously written ZERO there results a flux which is indistinguishable from that

of a ONE written on a previously unmagnetized area. This is also true when a signal is superimposed over a signal of the same polarity. Thus the process of erasing can be eliminated.

Description of the Write Amplifier

The purpose of the write amplifier is to transform logic pulses into current pulses which, when driven through the recording head of a magnetic drum system, record the data on the drum. A typical write amplifier is shown in Fig 7-3.

Theory of Operation

In order to write data on the magnetic drum it is necessary to produce magnetic flux which will magnetize the drum surface. This flux is generated by driving current pulses through an inductive coil of the magnetic head which is mounted close to the drum surface. The flux produced cuts the surface of the drum which is coated with a very thin layer of a ferro-magnetic compound which has a high magnetic retentivity.

The recording method used is known as the "return-to bias" method. In this method, the entire track beneath a head is first magnetized to saturation in one direction. Essentially, the track then contains all zeros. A logic pulse representing a ONE is recorded by passing a short current pulse through the head in the opposite direction causing a small segment of the magnetic surface

to be driven to saturation in a direction opposite to that of the original bias.

A supply voltage is applied at the center tap of the head coil so that the direction of magnetization may be controlled by choosing the branch of the head in which current is permitted to flow. The output stage of the write amplifier consists of two current switches which determine the magnetic polarity. When no writing is desired both switches are disabled.

The logic for these operations may be accomplished by using an inverter, two AND gates and two switches as shown in Fig C-2.

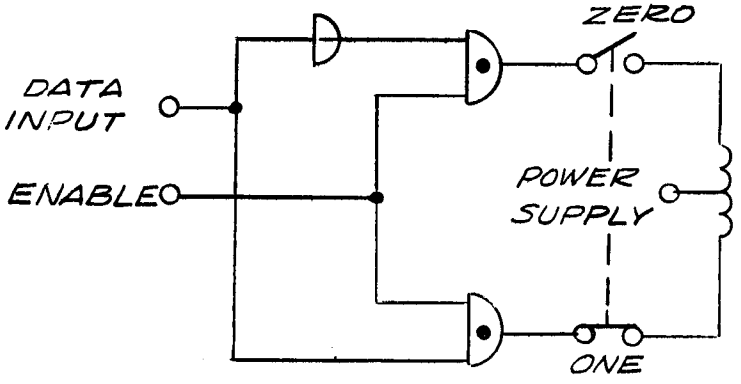


Fig C-2 Write Amplifier Basic Logic

The complete schematic is shown in Fig C-3.

A ONE at the data input is represented by OV. A ZERO by -10V. ENABLE ONE is represented by OV and DISABLE (ZERO) by -10V.

When a ZERO is present at the ENABLE, Q3 is turned off, which

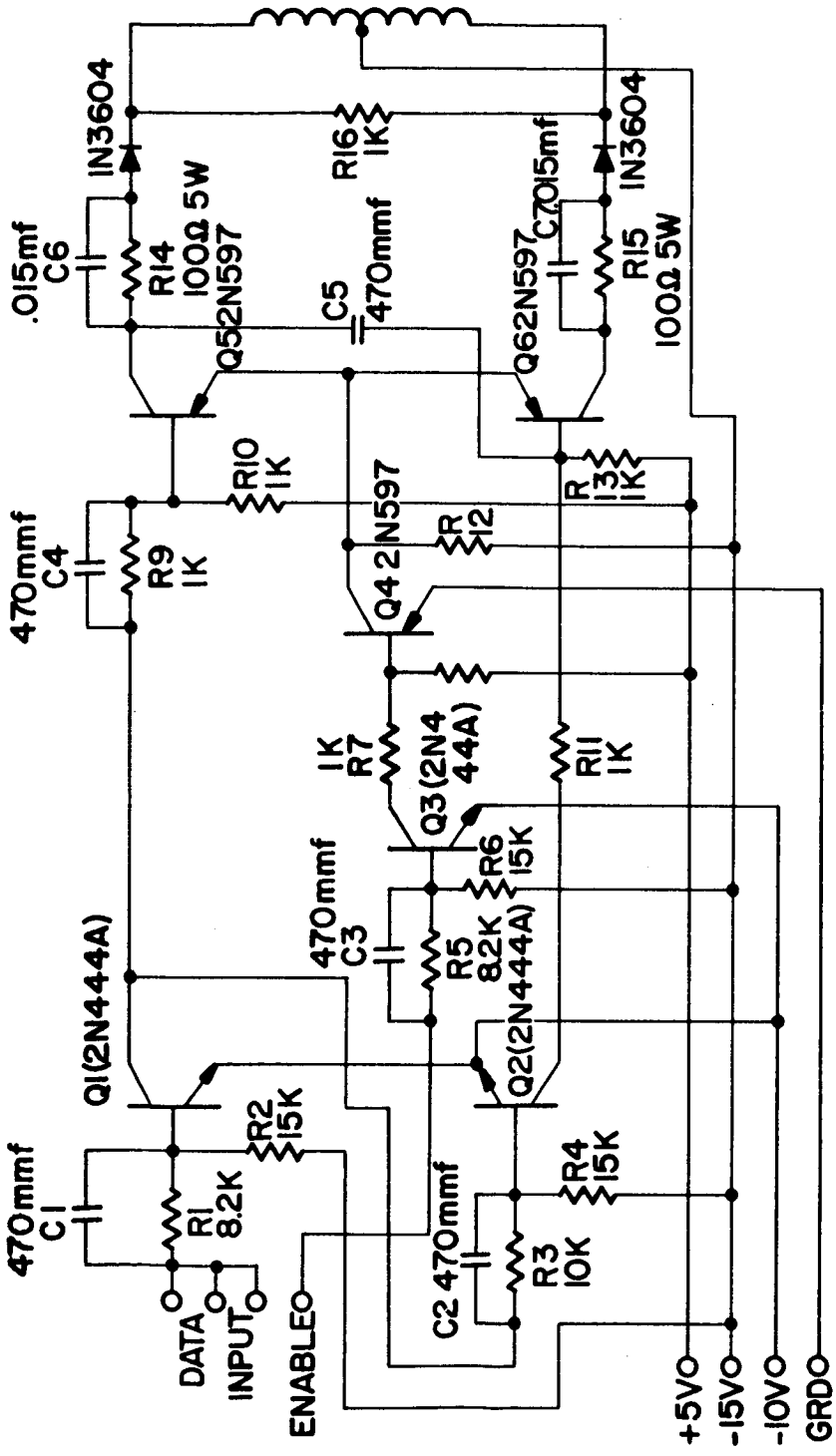


FIGURE C-3 WRITE AMPLIFIER SCHEMATIC

turns off Q4. With Q4 turned off the emitters of Q5 and Q6 are at-15V through R12, the same as the coil center-tap and no current flows in the coil regardless of the data input state. With a ONE on the enable, Q3 and Q4 are turned on bringing the emitters of Q5 and Q6 to OV.

With a ZERO on the data input, Q1 is turned off, as is Q5. Q2 is turned on by the voltage divider formed of R10, R11, R3 and R4. The collector of Q2 will be at -10 volts in the on condition and Q6 will be turned on provided there is a ONE on the enable input. With Q6 turned on current will flow through the ZERO side of the coil toward the -15V supply. This causes a logic ZERO to be recorded.

With a ONE on the data input Q1 is turned on and its collector goes to -10 volts turning Q2 off and Q5 on. Q2 turns Q6 off blocking the ZERO write current. Q5 allows current to pass through the ONE side of the coil, causing a logic ONE to be recorded.

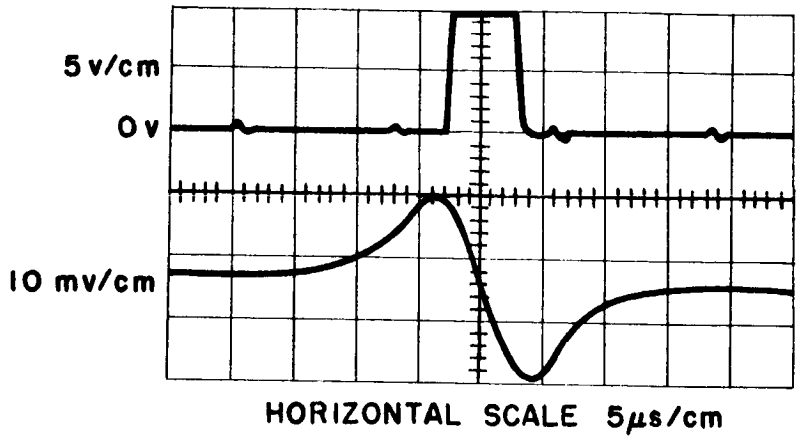
The L/R time constant of the coil plus the series resistor used to limit the coil current opposes a fast change in direction of the coil current. Speed up capacitors C6 and C7 decrease this time constant and give the current pulses a faster rise time.

The purpose of R16 and the diodes is to suppress any inductive spikes caused by cutting off the coil current sharply.

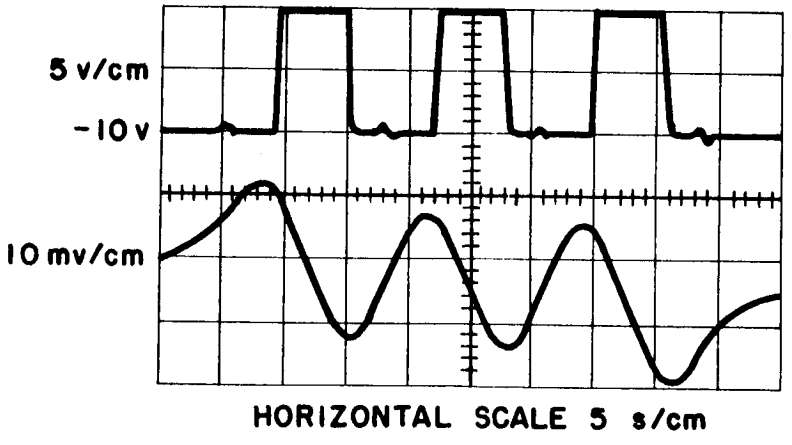
The playback signal associated with a logic pulse is shown in Fig C-4. It may be observed that the read back drum signal reaches a positive peak before the rise of the logic pulse that wrote it. The two waves are recorded on the same time base. It can also be seen that the read back signal is considerably longer than the logic pulse. Both of these factors are due to the "spreading" effect.

The spreading effect occurs because the recording head core gap is .001" and the head is mounted .001 from the drum surface. The magnetic field created by the current pulse fans out radially from the gap and the lines of force cut the drum surface on both sides of the head. During playback the magnetic flux from the drum induces a voltage in the coil each time it passes the head. This flux also fans out radially and a small induced voltage is created as soon as the gap cuts the most distant radial flux.

It may be seen by again referring to Fig C-4(a) that the read back signal increases as the magnetized segment approaches the head, returns to zero during the time that the magnetized segment is in saturation, is driven negative as the magnetization returns to bias, and again comes to zero since no lines are cut as the pre-biased surface passes. Because a very short write current pulse is used, and due to the head gap and displacement from the drum, the read back signal does not remain



(a) SINGLE PULSE



(b) PULSE TRAIN

FIGURE C-4 PLAYBACK PULSES

at zero after its positive excursion. It is being driven negatively immediately by the trailing return-to-bias edge of the recorded magnetic pulse. This accounts for its sinusoidal appearance.

When several pulses are written in close succession, the "crowding effect" occurs. This can be seen by referring to Fig (C-4)(b). The field of the second pulse being written causes the first to be less sharply defined and also reduced in magnitude. The writing of the third pulse effects the second in the same way. The leading edge of the first pulse and the trailing edge of the third pulse are not crowded, and induce normal playback.

Description of the Read Amplifier

The purpose of the Read Amplifier is to transform the low voltage playback signal induced in the read head of a magnetic drum system into a standard logic signal. A typical read amplifier is shown in Fig 7-4.

Theory of Operation

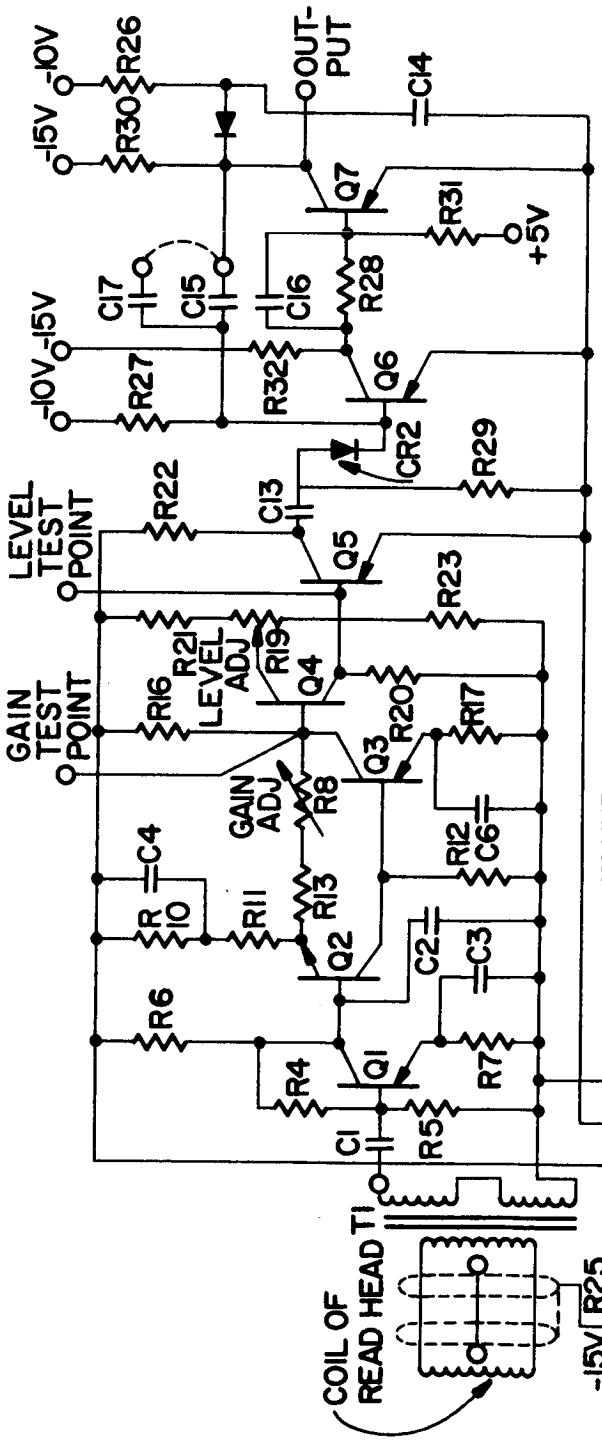
The recording of magnetic pulses and how these pulses induce a playback signal across the read head has been explained in the theory of operation of the write amplifier. It is the function of the read amplifier to amplify these playback signals, clip them, and to develop uniform logic pulses from them.

Since in this system, the read head is not the write head, different head to drum spacings will occur. Also, the gain of the heads varies from unit to unit. It is possible then that low gain units may not read low playback voltages and high gain units would falsely interpret low level noise as playback. Hence, a gain adjustment and a clipping level adjustment are provided.

A schematic of the read amplifier is given in Fig (C-5). The read head is connected to the amplifier by means of shielded cable. Common mode signals picked up by the leads are rejected by the use of an input transformer connected differentially.

The transformation of the playback signals into logic pulses may be accomplished in several ways. One way is to amplify the signals as they are, clip them, and use the positive portion of the wave to trigger a pulse shaping circuit. However, due to the "spreading effect" and the "crowding effect" it may be seen in Fig (C-4)(b) that the playback signals do not all rise uniformly nor are they all of the same amplitude. Clipping these signals all at the same d-c level would result in irregular time intervals in the output logic pulses. This irregularity would occur because an uncrowded pulse would reach that d-c level earlier than a crowded pulse.

It may be observed, however, that the slope of the line between the positive and negative peaks of each playback pulse



C_1	220 MMFD	Q_1 Q_3 Q_5	2N414	R_{11}	330
C_2 C_{16}	470 MMFD	Q_6 Q_7		R_{19}	1K Trimpot
C_3, C_4, C_9, C_{10}	IMFD @ 100WV	Q_2, Q_4	2N444A	R_{20}	5.6 K
C_6	.22 MFD@ 200WV			R_{21}	560
C_{11}, C_{12}	500 MFD@ 25WV	R_3 IK		R_{22}, R_{30}, R_{32}	1.5K
C_{13}	330 MMF	R_4, R_5, 22KK		R_{23}	680
C_{14}	0.1 MFD@ 100WV	R_6 6.8K		R_{24}	33
C_{15}	470 MMFD 5%	R_7 10K		R_{25}, R_{26}	100
C_{17}	330 MMFD 5%	R_8 25K	Trimpot	R_{27}	14.7K
CR2, CR3	IN 625	R_{10}, R_{12}, R_{13}	4.7K	R_{29}	2.2K
		R_{16}, R_{17} R_{28}		R_{31}	12K

FIGURE C-5 READ AMPLIFIER SCHEMATIC

is the same. Also, the slope is a maximum directly under the center of the logic pulse used to write it. For these reasons, the slope, first derivative, of the waveform is used to obtain logic pulses with regular time intervals.

The first stage of the read amplifier serves as a differentiating circuit as well as an a-c amplifier. Transistor Q1 has a very low a-c input impedance since its emitter resistor R7 is by-passed by capacitor C3 and the input is shunted by R4, R5 and R6. The output voltage of the first stage is equal to the input current times a constant, the constant being a function of the gain of Q1, the feedback of the circuit, etc. Since the input impedance of Q1 is very small, the current flowing out of the base of Q1 is determined by the value of C1. This current is a function of the first derivative of the voltage applied to C1 by the transformer. Therefore, the output voltage of the first stage is proportional to the first derivative of the input voltage.

The first stage is a current input stage. Due to its low input impedance very little voltage is developed at the base of Q1. Fig C-6 shows a playback signal on the primary of the transformer and its derivative at the collector of Q1.

The second and third stages act as an a-c amplifier. Variable resistor R8 in the feedback circuit acts as a gain control. Emitter by-pass capacitors are used in both stages to increase a-c gain. R11 provides some unbypassed emitter

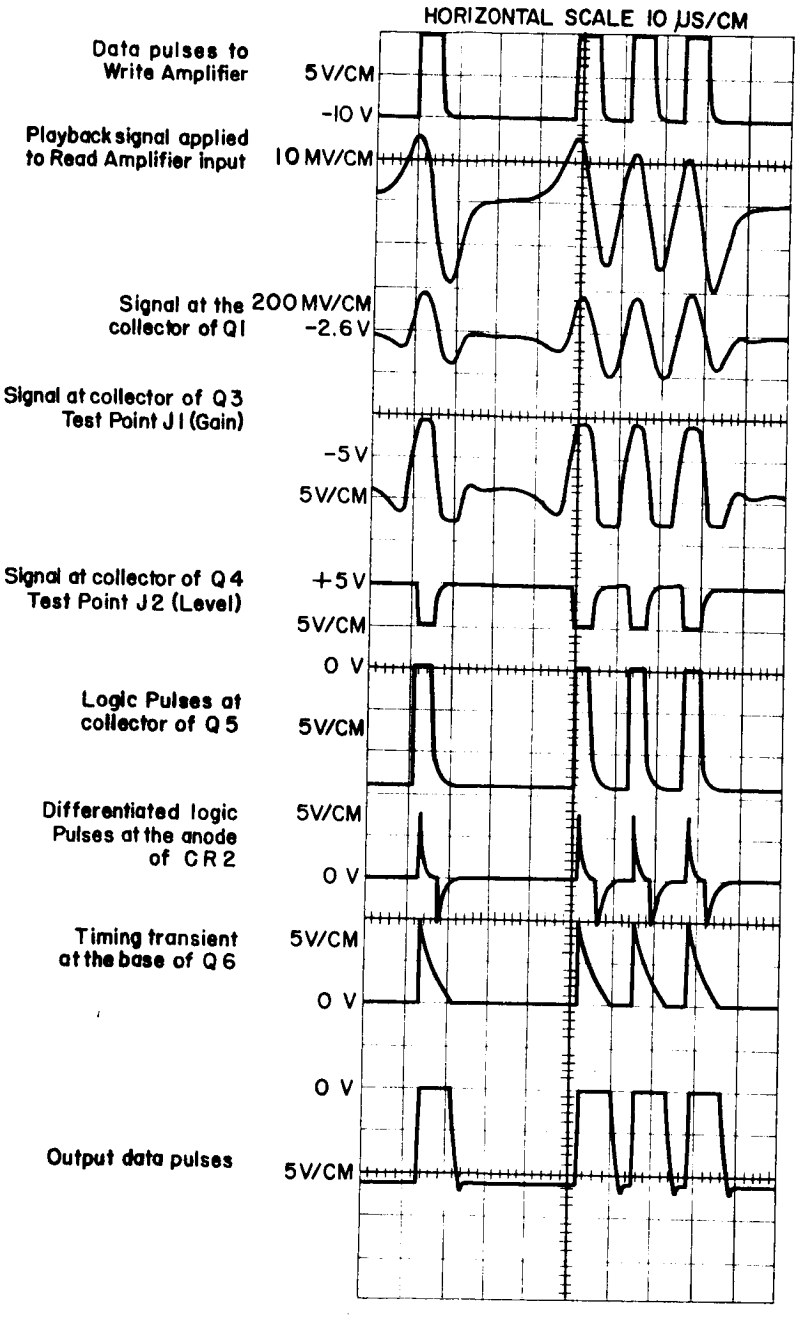


FIGURE C-6 READ AMPLIFIER WAVEFORMS

resistance in the second stage across which a-c feedback voltage is developed. Capacitor C2 provides a low impedance path for any high frequency noise to the +5V power supply thereby limiting the high frequency response of the amplifier.

The d-c gain of the amplifier is less than one. The emitter and collector resistors are approximately equal in the first three stages and the negative feedback further reduces the gain. Any d-c change at the base of Q1, Q2, or Q3 due to increased leakage current at high temperatures will appear at the collector of Q3 multiplied by the less than unity d-c gain.

The fourth stage is a discriminator or clipping stage. It acts as a switch and turns on when the base voltage goes more positive than the emitter. The emitter level is controlled by variable resistor R19.

With no input to the circuit the collector of Q3 is at approximately -8.6 volts. With playback signals applied to the input, the gain is adjusted so that the signals drive Q3 slightly into saturation in the positive direction, Fig (C-6). The positive peaks are cut off at -1 volt. R19 is adjusted so that the emitter of Q4 is at about -3 volts. Any signals which are not more positive than -3 volts are blocked by this stage. At this setting Q4 conducts for about 5μs when the signal amplitude reaches -2.7 volts at the collector of Q3. The collector

of Q4 goes from +5 volts to -0.3 volts at which point Q5 turns full on and Q4 collector voltage is clipped. The playback pulse appears at the collector of Q5 as a standard logic pulse (see Fig(C-6).

The playback signal may vary as much as 2 to 1 among different heads. If several different heads are to be read by the same read amplifier the gain should be adjusted so that the smallest signal to be read drives Q3 to saturation. This will cause the larger signals to drive Q3 further into saturation. They will also be wider at the clipping level. This causes the logic pulses at the collector of Q5 to be of different widths depending upon the amplitude of the playback signal.

To keep the pulse width constant, a pulse shaping circuit was added. This one-shot multivibrator times out a definite length pulse regardless of the pulse width from Q5. Two different pulse lengths are available. When a jumper is connector on the circuit card,, the pulse width is increased from 5μs to 9μs.

The one-shot multivibrator operates as follows: When Q5 is at a logic ZERO, -10V, Q6 is turned on by current through R27. The collector of Q6 is at 0 volts and the base of Q7 is positive due to R28 and R31. Therefore, Q7 is off and the output is -10V.(ZERO).

C13 differentiates logic pulses from the collector of Q5, Fig C-5. The positive going spike, caused by the leading edge of the logic pulse, goes through CR2 and turns Q6 off. Q7 is turned on since its base is negative due to R32, R28, and R31. The collector of Q7 goes to zero volts, a logic ONE. The collector of Q7 changed +10V abruptly. The voltage across a capacitor cannot change abruptly, therefore the base of Q6 increases abruptly by +10V holding Q6 off. However, the capacitor begins to discharge through R27. When the base of Q6 reaches 0- volts, Q6 turns on. Its collector goes to 0 volts and Q7 turns off. The collector of Q7 is pulled toward -15 volts by R30 but CR3 conducts when it reaches -10 volts and holds it there. The fall time of the output pulse is rather slow 2μs, because the timing capacitor must be discharged by R30 in parallel with any external load. The negative spike generated across C13 by the fall of the logic pulse back biases CR2 and does not appear at the base of Q6.

C14 and R26 form a filter for the ten volt power supply since high frequency noise on the -10V supply has a low impedance path through C15 to the base of Q6. This noise could accidently trigger the circuit if not filtered. The rise time of the circuit is 0.2μs, Fig C-6.

It may be observed from Fig C-6 that the data pulse from

the read amplifier lags the data input pulses by 4μs. Actually, the lag is 1/2 the width of the data pulse. The lag occurs because the output pulses are being generated by the first derivative of the playback signal, and this derivative signal peaks in the middle of the playback pulse.

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